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# HANDBOOK OF INSTRUCTIONS FOR MEC MODEL 78 RECEIVER REGISTER

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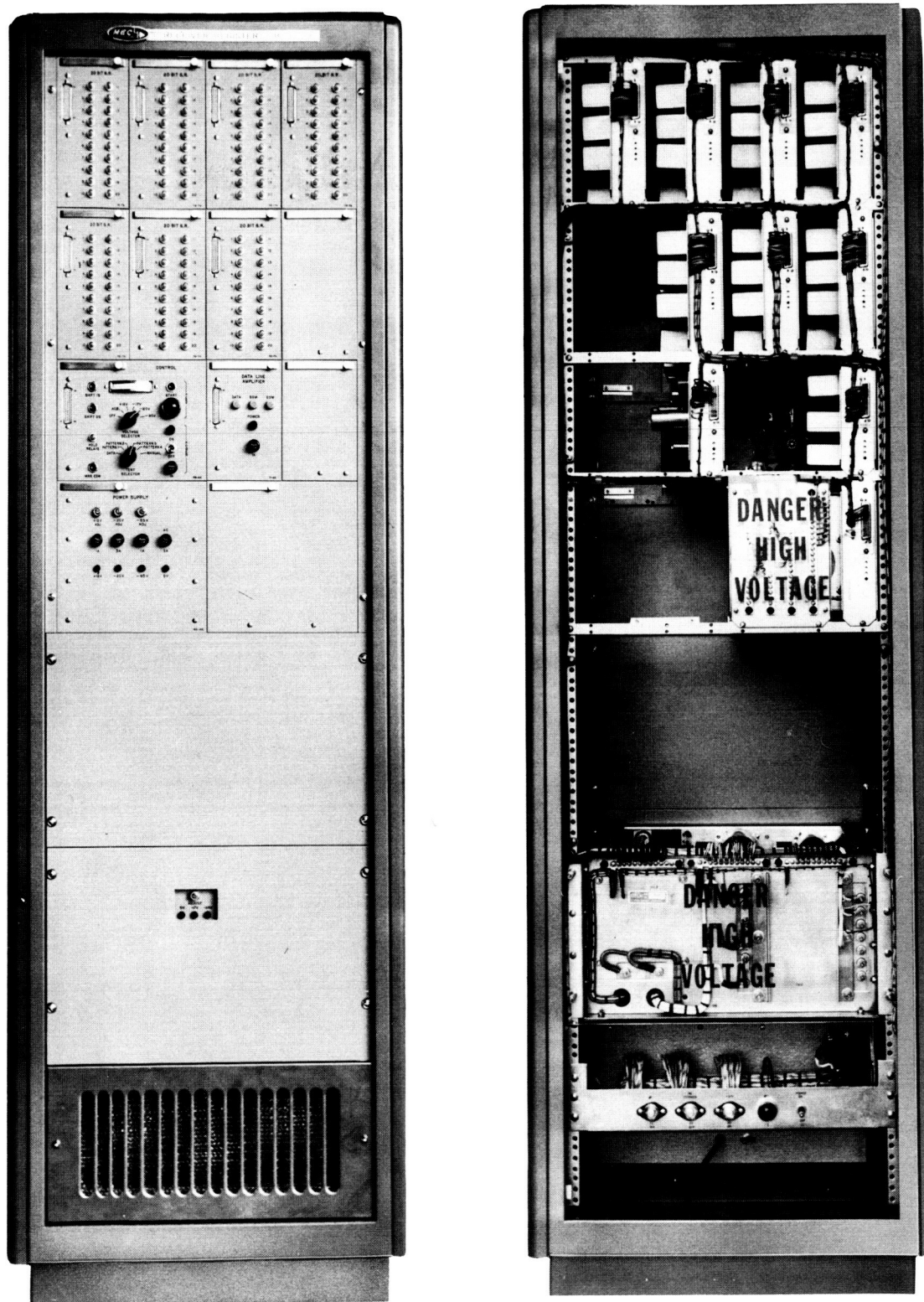


Figure 1-1. MEC Model 78 Receiver Register

## **CHAPTER I**

### **INTRODUCTION**

#### **1-1. PURPOSE OF THE EQUIPMENT.**

The Milgo Electronic Corporation (MEC) Model 78 Receiver Register is designed to accept up to 140 bits of digital data in serial form from a 3kc 600 ohm telephone channel, and to present these bits on 140 parallel output lines wherein the data of a given word is held until the next word has been accumulated and is ready for readout.

#### **1-2. SCOPE.**

This instruction manual describes the MEC Model 78 Receiver Register, designed and manufactured by MEC, for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

#### **1-3. PURPOSE OF MANUAL.**

This instruction manual is provided as an aid to better understanding of the operation and theory of the MEC Model 78 Receiver Register and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations. It is necessary that the operator, or any person involved in the operation of this equipment, thoroughly read and fully understand the contents of this manual.

## CHAPTER II

### GENERAL DESCRIPTION

#### 2-1. PHYSICAL DESCRIPTION.

The MEC Model 78 Receiver Register is contained in one standard MEC type 1007-41 rack, which is 74 1/8 inches high, 23 9/16 inches wide, and 22 inches deep. The weight of the entire rack, with chassis installed, is approximately 475 pounds. The individual chassis that make up the Register are of modular construction, and are held in place in the rack by a single locking handle. The chassis that are identical in type are interchangeable. Figure 9-1 represents a block diagram of the system.

#### 2-2. SIGNAL INPUTS.

The Receiver Register accepts tone bursts of a 2kc carrier, modulated at a 1kc rate, from a 3kc, 600 ohm communication line which has been equalized for a 1kc data bit rate. For proper operation, a data word consisting of from 1 to 140 bits must be followed by an End-of-Word (EOW) signal. The EOW signal is 9 cycles of the 2kc carrier (4.5 milliseconds). Input signals between -30 dbm and +10 dbm can be accepted. Minimum signal-to-noise ratio must be in the order of 3:1 in the band-pass range. Outside the band-pass range, noise will be attenuated at least 20 db per octave. The signal input enters on J16, on the connector panel toward the rear.

#### 2-3. SIGNAL OUTPUTS.

The Receiver Register has 140 output lines that are connected to J115, J116 and J117 on the connector panel. Output signals are as follows: a binary "1" is -17 volts  $\pm$  3 volts, and a binary "0" is 0 volts  $\pm$  .5 volts.

#### 2-4. ELECTRICAL LINE SPECIFICATIONS.

Line power input is at 120vac  $\pm$ 10%, single-phase 60 cps  $\pm$ 5cps, at approximately 15 amps. Connection is made at J15 on the connector panel at the rear of the rack.

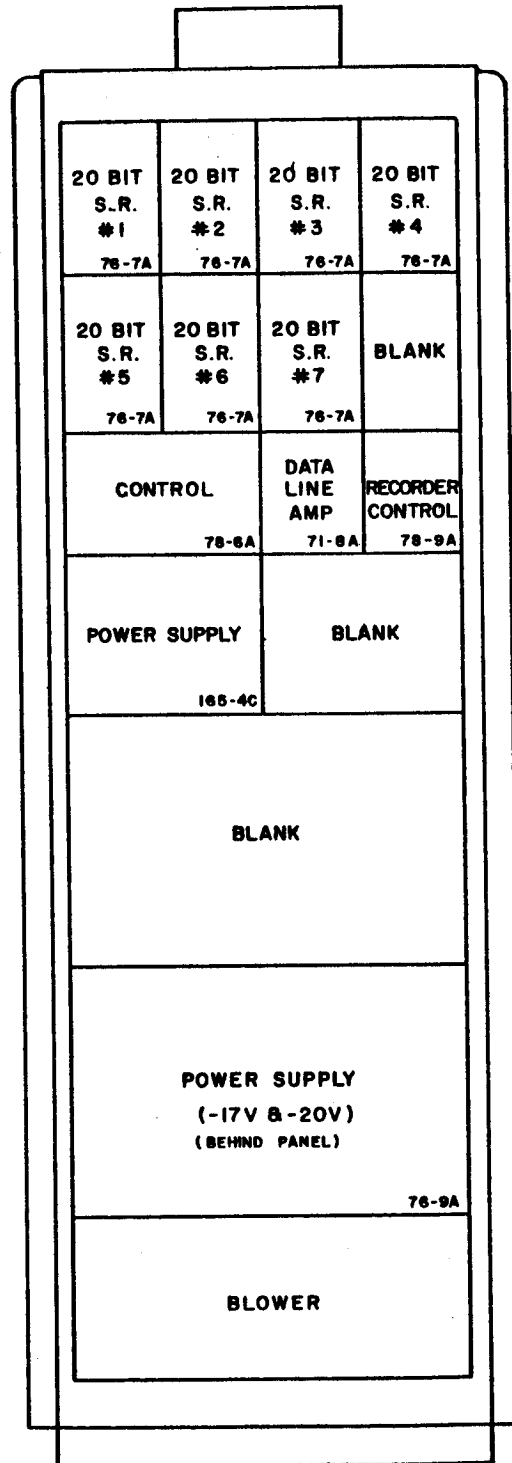


Figure 2-1. Assembly Arrangement, Model 78 Receiver Register

## CHAPTER III

### THEORY OF OPERATION

#### 3-1 GENERAL (Refer to Logic Diagram, Figure 9-2)

3-1.1 Three general modes of operation are possible in the MEC Model 78 Receiver Register - data, playback and test. In the data mode, data and EOW are received by the Data Line Amplifier, where they are changed into pulse form and sent to the Control chassis. One kc is generated in the Data Line Amplifier, and sent to the Control chassis for timing purposes. Another output of the Data Line Amplifier provides for the recording of the data on tape. In the playback mode, data from the tape recorder is inserted into the Data Line Amplifier and the Receiver Register functions just as in the data mode. Indicator light I901 mounted on the Recorder Control chassis 78-9A is on during the playback mode to warn the operator he is not in the operate (or data) mode. In a test mode, (pattern 1, 2, 3, 4, or manual), the Data Line Amplifier is disconnected from the Control chassis, with data, EOW, and 1 kc being generated in the Control chassis. Four test data patterns are available, all at a 1 kc bit rate. A manual type of test mode is also available for manual insertion of the data pattern desired, plus a manual insertion of EOW. Indicator light I601 is on in all test patterns, to warn the operator that he is not in the operate mode.

3-1.2 Data Mode - This is the mode for actual operation of the Model 78. As data is received from a telephone line, it is fed into the Data Line Amplifier, changed to pulse information, and sent to the Control chassis. A 1 kc sine wave is also generated in the Amplifier chassis and fed into the Control chassis. To insure proper synchronization of the Model 78 with the equipment that is transmitting data to it, the incoming data bits are used to sync the 1 kc oscillator. The EOW tone burst is detected by the Data Line Amplifier, and sent to the Control chassis as a pulse. The Control chassis inserts the data into the core shift registers, and uses the 1 kc oscillator to time drive pulses sent to the Shift Register chassis. Upon receipt of the EOW pulse, a pulse is generated that opens a gate on the shift register, and allows the data to be shifted (in parallel) out of the shift registers and into storage flip-flops which drive the output lines. In this mode, anywhere from 1 to 140 bits may be received by the register. When the information is transferred out of the shift register, 140 bits are transferred, regardless of how many bits are received. This means that readout equipment must be terminated at the correct pins of J115, J116 and J117, in order to correctly interpret the information. For example, if out of 140 possible bits only 100 are significant, then 40 bits that are available for the transfer are inconclusive or meaningless. Since the outputs of the Model 78 Receiver Register often will be used to drive digital-to-analog converters, a D-A Hold signal is generated. This signal allows the D-A converter to be put in a hold cycle while the data is being changed.

3-1.3 Playback Mode - During the playback mode, data which had been previously recorded on tape when the Receiver Register was operating in the data mode, is used as the input to the Data Line Amplifier. Except for the source of data, the Receiver Register functions just as in the data mode. The playback mode is included to enable the re-running of previously received data through the Receiver Register for further evaluation.

#### 3-1.4 Test Mode

3-1.4.1. Pattern 1, 2, 3 and 4 - In these modes, the Model 78 operates from internal test circuitry, with the Data Line Amplifier disconnected from the Control chassis. For timing purposes, a 1 kc signal is generated by a free-running multivibrator, and data is synthesized by a counter (in the 1-0 or 0-1 pattern), or a Schmitt trigger (in the all 1's). EOW is generated periodically by a free-running multivibrator, and is timed so that more

than enough bits enter the register to fill up all 140 storage locations before a command is given to transfer.

3-1.4.2 Manual - In this mode data may be inserted manually in any pattern desired. S603 (Shift 1's) is pressed for a "1" insert, and S604 (Shift 0's) is pressed for a "0" insert. When EOW is desired, S605 (MAN EOW) is pressed. It must be kept in mind that when EOW is generated in the Manual mode, the last six data bits inserted are still in the Control chassis, and have not been shifted into the Shift Register chassis. This is because the Model 78, when in the Data mode, must allow for the delay between the last data bit and the detected EOW signal from the Data Line Amplifier.

### 3-2 DATA LINE AMPLIFIER, MEC Model 71-8A (See Schematic in Appendix)

The Data Line Amplifier chassis receives the modulated tone bursts, and converts these into data bits and EOW bits. These bits are then fed into the Control chassis. A complete discussion of the Model 71-8A Amplifier is contained in the Appendix of this manual.

### 3-3 CONTROL CHASSIS, MEC Model 78-6A (Figures 9-3 and 9-8)

In order to understand the operation of the Control chassis, reference should be made first to the wave form diagrams (Sheets 7 and 8 of the DLA writeup in the Appendix) of the Data Line Amplifier outputs.

3-3.1 It should be noticed that data pulses appear approximately 150 microseconds after the lkc has crossed the zero point while going in the positive direction. Also, a false data bit appears after the last data bit, and 4 milliseconds before the EOW bit appears.

3-3.2 When the Model 78 is in the OPERATE mode, a lkc sine wave comes into the Control chassis, and is squared in N606, a Schmitt trigger. N606 switches at -3 volts, and the output (pin 7) is in phase with the input (pin 3). That is, when pin 3 is positive-going and crosses -3 volts, pin 7 goes from -20 volts to 0 volts. When pin 7 of N606 goes positive, it triggers N607, a 500-microsecond one-shot. When N607 is fired, pin 5 goes from 0 volts to -20 volts and stays there for 500 microseconds, after which it returns to 0 volts. The positive-going voltage is a-c coupled into an "or" gate consisting of CR608, CR609 and R618, and triggers N608, a 10 microsecond one-shot. CR608, R617 and R266 provide a 2 volt noise bias. When N608 fires, pin 7 goes from -20 volts to 0 volts, which is the trigger for core driver N609. The output of N608 is also fed into the Shift Register chassis for triggering the respective core drivers (See Figure 9-8(b)).

3-3.3 As can be seen from Sheet 8 (DLA writeup in Appendix), a data bit comes into the Control chassis approximately 200 microseconds after the lkc has switched the Schmitt trigger. This data bit triggers N605, a 20 microsecond one-shot that inserts a "1" into core M601. A 2 volt noise bias is provided for the core by R606, R616 and CR 607. R605 is used as a current-limiting device for the auxiliary winding of the core. An important point to remember is that, although data arrives 250 microseconds after the Schmitt trigger has switched, N607 delays shifting the cores for 500 microseconds. This means that data is inserted, then shifted 200 microseconds later.

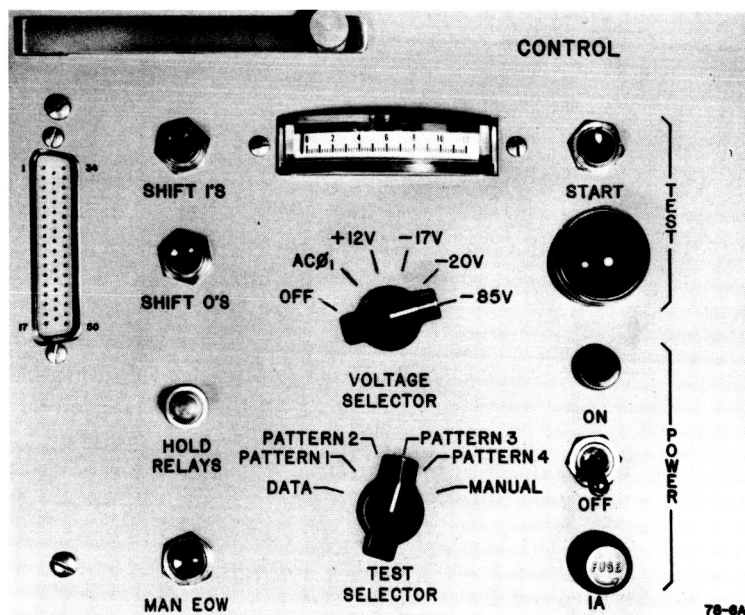


Figure 3-1. Control Chassis



3-3.4 When EOW occurs, a false data bit comes to the Control chassis, followed by an EOW pulse 4 milliseconds later, as seen in the pulse diagram. This false data bit is 1 millisecond behind the last bit of actual data. This means that when the false bit is inserted in M601, the last data bit is in M602. If we call the time of insertion of the false data bit  $T_0$ , then at  $T_0 + 200$  microseconds, the false data bit is shifted to M602. At  $T_0 + 1.200$  milliseconds it is shifted to M603, and at  $T_0 + 3.200$  milliseconds it is shifted into M605. At  $T_0 + 4$  milliseconds, however, the EOW bit has entered the chassis, triggering N613, a 1-millisecond one-shot. When N613 is triggered, pin 7 goes from -20 volts to 0 volts, and triggers N614, a 5-millisecond one-shot. When N614 fires, pin 7 goes from -20 volts to 0 volts. This level is inverted in N618, and goes to a D-A Converter for opening the hold relays (See Figure 9-8(a)). At  $T_0 + 4.200$  milliseconds, the false data bit was shifted to M606, which means that the last data bit is now inserted in the 20-Bit Shift Register, in proper place for readout (See Figure 9-8(c) for wave form of data being inserted into the Shift Register chassis). At  $T_0 + 5$  milliseconds, N613 times out, and pin 5 goes from -20 volts to 0 volts. This triggers N615, a 10-microsecond one-shot. When N615 fires, pin 7 goes from -20 volts to 0 volts and triggers N616. When N616 fires, pin 7 goes to 0 volts and is sent to the Shift Register chassis, where it opens a readout gate and resets the readout flip-flop. At  $T_0 + 5.01$  milliseconds, N615 times out, and pin 5 goes from -20 volts to 0 volts. This level goes through N618, an emitter-follower, and is a-c coupled to N608 through the "or" gate previously mentioned. N608 then sends a pulse to the Shift Register chassis to trigger the core drivers, and the data is transferred. Twenty microseconds later, N616 times out, and the readout gate is closed. N614 then times out and the hold relays in the associated D-A Converter are closed. The Model 78 Register is then ready to repeat the cycle.

3-3.5 A system for monitoring the d-c power supplies is also incorporated into the Control chassis. MV601 is a 1.2 ma full-scale deflection milliammeter, mounted on the panel, that can be switched in series with each supply. A resistor is also placed in series with each supply to permit MV601 to perform the function of a voltmeter. Thus, when the current through the meter is 1.0 ma, the supply is correctly adjusted. The face of the meter is calibrated from 0 to 12; therefore, a reading of 10 indicates a current flow of 1 ma.

### 3-4 TEST MODE

#### 3-4.1 General

3-4.1.1 In all test modes, date, EOW and shifting is controlled internally by the Control chassis when in patterns 1, 2, 3 and 4. Shifting is timed by a free-running multivibrator, at 1kc, and EOW is generated once every 350 milliseconds by another free-running unit. In all test modes, an indicator lamp 1601 serves as visual warning to the operator.

3-4.1.2 N601, along with R609, R610, R611, C602 and C603 is a 1kc multivibrator. R610 is a variable resistor, used to adjust the timing of the multi. The 350 millisecond multivibrator is actually two one-shots, N610 and N611 hooked back-to-back. When N610, a 100 millisecond multi fires, pin 5 goes to -20 volts. 100 milliseconds later, pin 5 returns to 0 volts. The positive-going pulse triggers N611, a 250 millisecond multi. Pin 5 of N611 goes to -20 volts until it times out, then returns to 0 volts and triggers N610. Neither the 1kc multi nor the 350 millisecond multi are self-starting. When in patterns 1, 2, 3 or 4, pressing push-button S602 (TEST START) sends a positive pulse to both multis and starts them. This switch is disconnected in both the DATA and MANUAL positions of the Test Selector switch. Also, in these modes, a positive voltage is applied to pin 2 of N601 to keep it from oscillating.

3-4.2 Pattern 1 (All 1's). In this pattern, the output of the 1kc oscillator is fed into N602, a Schmitt trigger, for squaring. The output of N602 is fed into N606, where it is operated on exactly as the incoming 1kc was handled in the Data mode. The output of N602 also is fed into N603, a counter, and into the data inserter one-shot, N605. When pin 7 of N602 goes positive, one-shot N605 is triggered, a one is inserted in M601, and is shifted 500 microseconds later (the 500 microsecond delay is the result of the delay of N607). This cycle is repeated every millisecond, so ones are being inserted constantly. Concurrently with this, the 350 millisecond oscillator is running. If reference is made to the schematic of a TN28 (Appendix) it will be seen that there is a diode in series with pin 3. In this Control chassis, the diode in N604 is used with R625, R629 and C605 to form an "and" gate. When pin 7 of N611 is at -20 volts, pin 3 of N604 is at -20 volts. Since the cathode of the diode in N604 is clamped to -.3 volts, the diode is back-biased by 20 volts. When pin 5 of N603 goes positive, it swings approximately 18.5 volts, or from -19 volts to -.5 volts. This swing is a-c coupled by C605 to pin 3 of N604, and is not enough to make the series diode in N604 conduct. When pin 7 of N611 is up, it sits at approximately -.5 volt. Pin 3 of N604 then sits at approximately -2 volts. Then when pin 5 of N603 goes positive, the series diode in N604 conducts and N604 changes state. When N604 changes state, pin 8 goes from 20 volts to 0 volts and inserts an EOW pulse in N613, which is then handled as the EOW pulse from the Data Line Amplifier, handled in Data mode. It is important to note that EOW is generated only once every 350 milliseconds. After N604 generates the EOW pulse, it waits for 250 milliseconds and is then reset on pin 7 by the positive going pulse from pin 7 of N610. Even though N603 is counting continuously after N604 is reset, pin 7 of N611 went to -20 volts at reset, and will not allow N604 to be set for another 100 milliseconds.

3-4.3 Pattern 2 (1-0). In this pattern, the chassis generates "1's" and "0's" alternately. The first bit generated, however, is not necessarily a "1". What is important is that the last bit before EOW is a "0". Then, if more bits are generated than is needed to fill up the Shift Register, the excess bits will be dumped, and at EOW, the correct pattern will be in the cores.

In this pattern, data is not the output of N602, as it was in the all ones pattern. Instead, it is counted down by two in N603. Since the shift rate has not changed, every other bit inserted is a "1". The "and" gate previously mentioned insures that the last bit entered

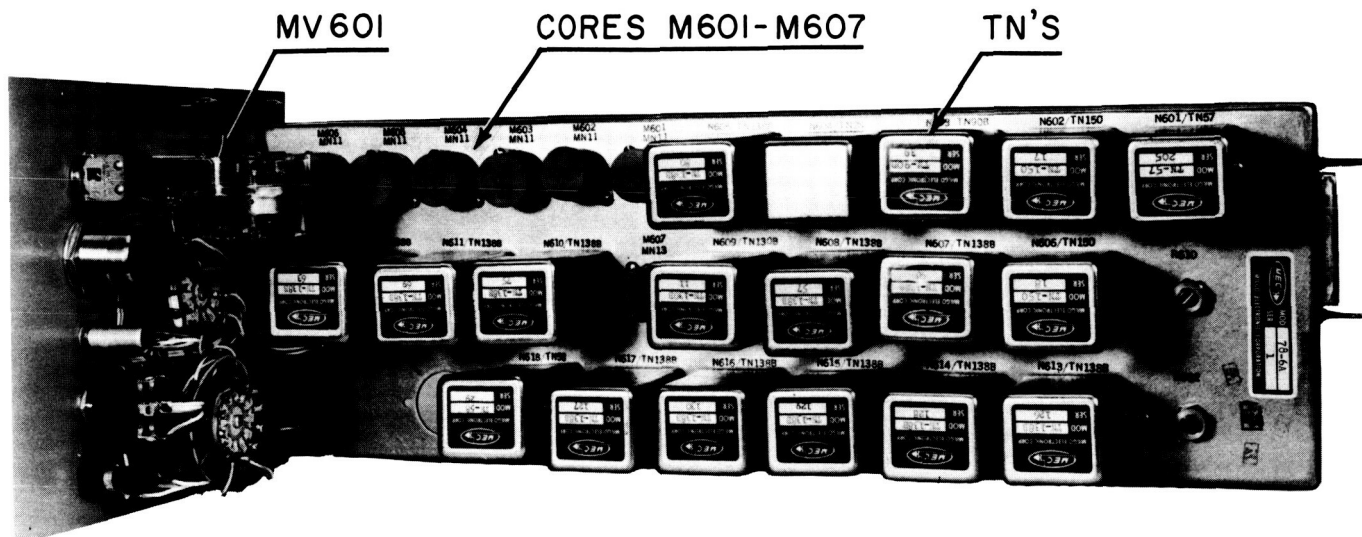


Figure 3-2. Control chassis Assembly, showing components.

is a zero. After pin 7 of N611 goes to 0 volts, the next positive going pulse of N603 inserts a data one and sets N604, which inserts an EOW pulse in N613. Since this data bit coincides with EOW, it looks like the false bit that comes from the Data Line Amplifier, and which has been shifted to M606 when the shift registers dump. Since the bit preceding it was a zero, and this zero is now in the last core, the test pattern was a 1-0.

3-4.4 Pattern 3(0-1). The operation of the Control chassis in this mode is very similar to the operation in pattern 2. However, data is taken from pin 8 of N603, instead of pin 5. The output of pin 8 is the opposite of pin 5, being 0 volts when 5 is at -20 volts, and -20 volts when pin 8 is at 0 volts. Since the rest of the chassis is operating the same, the data pattern is received, and a 0-1 pattern is the result.

3-4.5 Pattern 4 (All "0"s). In pattern 4 the chassis operates as it does in the preceding test patterns, except for the data insertion. In this pattern, there is no input to N605, hence no 1's are inserted, and an all 0 pattern is the result.

3-4.6 Manual. In the manual test mode, the 1kc oscillator is turned off. This is done by applying 12 volts to pin 2 of N601, which is the base of one of the two transistors that make up the oscillator. Since the chassis is in manual, a shift is desired only when the SHIFT 1'S (S603) or SHIFT 0'S (S604) button is pushed. Also, EOW is inserted only when the MAN EOW button is pushed. For data insertion, either S603 or S604 is pushed. If S603 is pushed, a positive going pulse is applied to pin 3 of one-shot N612. Pin 7 then goes to zero volts and is a-c coupled to N605 through S601B. At the same time, pin 7 of N612 also triggers N606 through S601C. Thus a 1 is inserted and, 500 microseconds later is shifted. If S604 is pushed, a positive going pulse is applied to N606, but because of the blocking action of CR612, (pin 7 of N612 is at -20 volts) the one-shot N605 is not triggered. In this manner, a zero is inserted, then shifted.

3-4.7 . To generate an EOW pulse, S605 (MAN EOW) is pressed. This applies a positive going pulse in pin 3 of one-shot N617. Pin 7 of N617 then jumps from -20 volts to 0 volts and triggers N613 through S601D. This inserts an EOW pulse and the shift registers dump as previously explained. A point to remember here is that when MAN EOW is pressed, the last data bit inserted is in M602 and will not be in the Shift Registers.

### 3-5 20 BIT SHIFT REGISTER, MEC Model 76-7A (Figure 9-5)

3-5.1 The function of the 20-Bit Shift Register is to accumulate data in a serial form and transfer it into a parallel form. The data is received serially and stored in 20 magnetic cores (M701 through M720). Upon command, the data is read into 20 flip-flops (N701 through N720), and will remain there while new data is being shifted through the cores M701 - M720.

3-5.2 A more detailed description of operation is as follows: In the Control chassis, two pulses are derived from the EOW pulse; a flip-flop reset trigger (from -20 volts to 0 volts, width 30 microseconds) and a read gate (from -20 volts to 0 volts, width 30 microseconds). The flip-flop reset trigger is capacitive coupled through C701 to pin 3 of a one-shot (N723) with emitter-follower output. The theory of operation of TN's used in this equipment is explained in detail in the Appendix.

3-5.3 When pin 3 of N723 goes positive (from -20 volts to 0 volts), the output pin 7 goes positive (from -20 volts to 0 volts, width approximately 5 microseconds). Pin 7 of N723 is capacitive coupled through C702 to pin 5 of all the flip-flops N701-N720. Pins 5 of N701-N720 are biased at -7 volts (R721 and R722). Therefore, as pin 7 of N723 goes positive, pin 5 of all the flip-flops goes positive also (from -7 to above 0 volts), resetting all the flip-flops to the "0" state. The "states" of the flip-flops (TN 144) are defined as follows: When pin 8 is at 0 volts, the flip-flop is in a "0" state; and when pin 8 is at -17 volts, the flip-flop is in a "1" state.

3-5.4 At the same time that the flip-flop reset trigger enters the Shift Register, a read gate (from -20 volts to 0 volts, width 30 microseconds) enters pin 2 of an emitter-follower (N722). The output of N722 goes to pin 5 of all cores M701-M720, and is called the "flip-flop-gate". When pin 2 of N722 goes positive, pin 5 of all cores goes positive from -20 volts to -2 volts (see Figure 9-8(d)). R727 and R728 are used to give a -2 volt noise bias when the gate is open. Since the gate raises pin 5 of M701-M720, subsequently pin 4 of M701-M720 rises to -2 volts, and the flip-flops will not trigger. A voltage pulse equal to or greater than 0 volts must be present at pin 3 of the flip-flops in order for a change of state to occur.

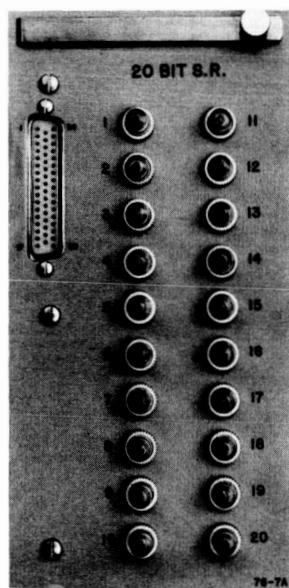


Figure 3-3. 20-Bit Shift Register Chassis.

3-5.5 The next shift pulse (-20 volts to 0 volts, width 40 microseconds) will cause the state of the core to be read out into the flip-flops. This shift pulse will be 10 microseconds from the leading edge of the read gate. Since the flip-flop gate is 30 microseconds wide, this shift pulse will cause core readout to occur approximately in the middle of the gate. Assuming that there was a "1" in the core, a 10 microsecond pulse (of 5 to 8 volts in amplitude) will be superimposed on the flip-flop gate at pin 4 of the cores, causing pin 3 of the flip-flop to go positive enough to set the state of the flip-flop to a "1".

3-5.6 If there was a "0" in the core, only the flip-flop gate will be present at pin 4 of the core; consequently, pin 3 of the flip-flop will go positive to only -2 volts, which is not sufficient to change the state of the flip-flop. Since the flip-flop is initially reset to the "0" state, and this state remains unchanged if the core is in the "0" state, effectively one may say that the data in the core has been transferred to the flip-flops. The states of the cores are determined by the data which is read in serially. The serial data read in and the core shift pulses both occur at the same time, and their repetition rate is 1000 pps.

3-5.7 Pin 8 of M701 is the data input. Pin 9 of M701 is directly coupled to pin 8 of M702, and pin 9 of M702 is directly coupled to pin 8 of M703. This is repeated from M703 through M720, and constitutes the serial read-in arrangement. Since all pin 5's of the cores are connected together, the flip-flop gate occurs at all cores simultaneously, and the data is read out on pin 4 of the cores to pin 3 of the flip-flops, in parallel. Operation of the core string is explained in detail in the Appendix. N721 is a core driver, operating with a blocking oscillator core (M721).

3-5.8 The data in the flip-flops is read out continuously except for an interval of approximately 10 microseconds per word (see Figure 9-8(e)). This is the time between reset period and that space when the new data is read out of the cores. Each flip-flop (N701 through N720) has an indicator light associated with it (DS701-DS720), to indicate the state of the flip-flop. When a flip-flop is in the "1" state, its respective indicator will be on, and when a flip-flop is in the "0" state, its indicator will be off. The lights have been reverse biased at -2 volts by CR701-CR703 and by R723, to insure that the lights will be off when the flip-flops are in the "0" state. C704, C705 and C707

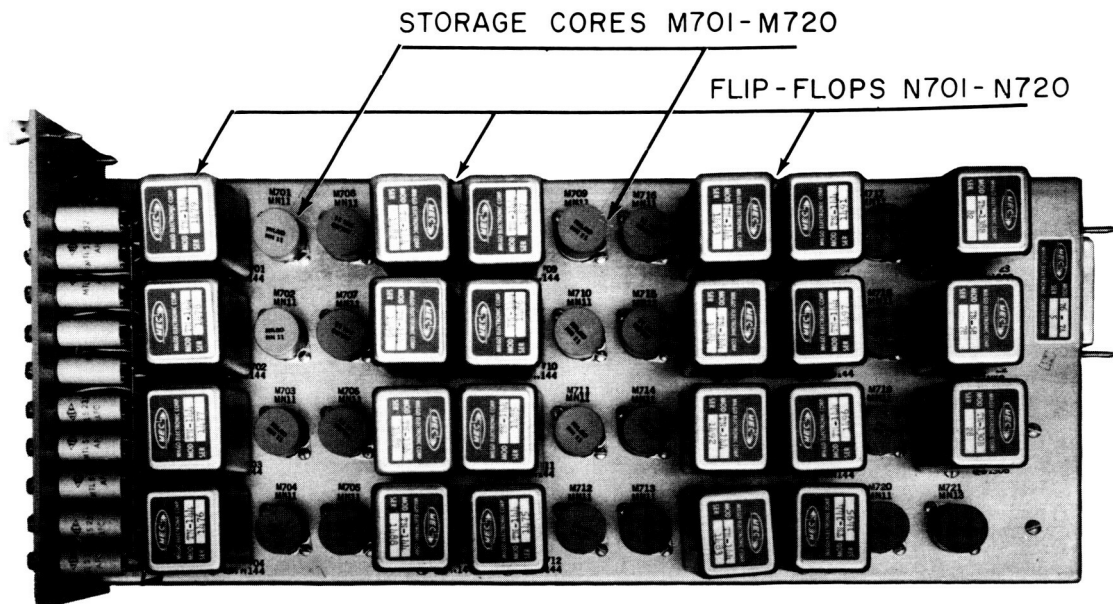


Figure 3-4. 20-Bit Shift Register Assembly

are used as filter capacitors between the power voltages.

3-5.9 The 20-Bit Shift Register has a building capacity, in that any number of the units can be connected in series, to permit the use of any number of bits to a word.

### 3-6. RECORDER CONTROL CHASSIS, MEC MODEL 78-9A (Figures 9-9 and 9-10)

The Recorder Control chassis contains a two position switch with OPERATE and PLAYBACK positions. The Receiver Register may function either in the data mode or the test mode depending upon the position of the Control chassis selector switch. During the playback operation, the selector switch of the Control chassis must be in the DATA position. With the Recorder Control switch in the PLAYBACK position data from the tape recorder is fed into the data input lines of the Data Line Amplifier. Indicator lamp I901 is on during the playback operation to warn the operator he is not receiving data from the transmission line.

## CHAPTER IV

### OPERATION

The following procedure is a series of steps to be taken in setting up and operating the Model 78 Receiver Register:

- a. Ensure that a-c power is entering the rack through the input power connector, J15, and place S1 the base switch, in ON position. The indicator light should come on.
- b. Place the POWER switch (on CONTROL Chassis) in the ON position. The POWER ON indicator should light.
- c. By using the VOLTAGE SELECTOR switch and panel meter, check all d-c power supply voltages. All should read between 9.5 and 10.5.
- d. Select the test pattern (all 1's) with the TEST SELECTOR switch. The red TEST lamp should come on.
- e. Press TEST START pushbutton. All Shift Register panel bit lights should come on. Indicator light HOLD RELAYS on the Control panel should flicker at approximately 3cps. It is best to observe the D-A hold-relays output pulses at panel test jack TJ601-#16 with an oscilloscope. Pulses should be -17 volts  $\pm$  3 volts. Pulse width should be 5 millisecond,  $\pm$  .5 milliseconds.
- f. Check flip-flop outputs. With normal output load connected, the output can be monitored at pins 1-20 on the panel test jack (TJ 701) on each Shift Register with an oscilloscope. An output level of -7 volts  $\pm$  .5 volts represents a "0". Flip-flops should be reset at EOW time and set approximately 10 microseconds later. A more rigorous check may be run by removing the normal output loads and substituting a test cable terminated on a terminal board. See Chapter 8, Wire List, for pin connections. Load each flip-flop in turn, and observe the output for the proper levels.
- g. Select operate (DATA) mode with the selector switch. TEST indicator (I601) goes out. The Model 78 is now ready to operate.



## CHAPTER V

# INSTALLATION

### 5-1. PHYSICAL PLACEMENT

The physical installation of the Model 78 Receiver Register should be such as will properly fulfill all the requirements of stability, weight and ease of servicing as are outlined in those chapters dealing with such specifications. Thus, in Chapter 2, the gross weight, input and output terminals and other factors should govern the placement or positioning of the equipment. Leveling of the Register is not excessively critical, only dictated by the ordinary requirements of stable flooring. The base may be fastened to lugs embedded in the concrete; or some cleat arrangement may be fashioned, if so desired. Because of some potentiometer and oscillator slug adjustments which may be necessary on certain chassis, and which are mentioned in Chapter 6 and in the Appendix, it is necessary to allow clearance for swinging open the rear rack door. With some chassis units, it may be found easier to remove a blank panel in front in order to reach such adjustment points. In any case, caution must be observed in the vicinity of high voltages, as may be the case near power supplies.

### 5-2. POWER INPUTS

Power input requirements are mentioned in some detail in Chapter 2, and wire sizes for the rack wiring are given in the Wire List, Chapter 8. Note also, as is mentioned in Chapter 4, that there is a main power switch, S1, at the rear connector panel in addition to the one on the front Control panel.

## CHAPTER VI

# MAINTENANCE

### 6-1. PREVENTATIVE MAINTENANCE

Preventative maintenance is recommended for the following parts of the equipment:

- a. The Blower filter should be removed and cleaned in a solution of warm water and detergent at least every 30 days.
- b. The various electronic tubes should be tested periodically.

No other preventative maintenance is recommended.

### 6-2. MALFUNCTIONS

Malfunctions of individual parts are to be expected and can be located by troubleshooting using common test equipment (voltmeters, ohmmeters, ammeters, oscilloscopes, etc.). Many of the malfunctions can be located by merely observing the many neon lamps located on the front panels.

### 6-3. ADJUSTMENTS

6-3.1 Control Chassis - There are two adjustments to be made in the Control Chassis. One is an adjustment of R610, which adjusts the frequency of the 1kc oscillator used in the test modes. While observing the waveform on pin 7 of N602 with an oscilloscope, R610 should be adjusted to provide approximately 1kc output. The other adjustment is an adjustment for the delay time of N613. R632 should be adjusted until this delay time is 1 millisecond, as observed with an oscilloscope on pin 7.

6-3.2 Data Line Amplifier - The adjustment procedure for the Data Line amplifier is discussed in detail in the Theory of Operation Chapter.

6-3.3 The various adjustments that have been discussed in this instruction manual should be checked periodically to insure their accuracy.

## **CHAPTER VII**

### **PARTS LIST**

The MEC Model 78 Receiver Register consists of the following assemblies:

Quantity	Assembly
1	MEC Model 71-8A Data Line Amplifier
1	MEC Model 78-6A Control Chassis
7	MEC Model 76-7A 20-Bit Shift Register
1	MEC Model 165-4C Power Supply
1	MEC Model 76-9A Power Supply
1	MEC 78-1AAA Connector Bracket
1	Blower
1	MEC Model 78-9A Recorder Control Chassis



1 ITEM NO.	2 REFER. DESIG- NATOR	3 CLASS	4 STOCK NO.	5 MFG. AND PART NO.	6 DESCRIPTION							7 UNIT PER ASSY.	8 PROCURE- MENT CODE
					1	2	3	4	5	6	7		
6-26	M607			MEC MN-13							CORE, Magnetic	1	
6-27	N601			MEC TN-57							TRANSISTOR NETWORK	1	
6-28	N602 N606			MEC TN-150							TRANSISTOR NETWORK	2	
6-29	N603			MEC TN-90B							TRANSISTOR NETWORK	1	
6-30	N604			MEC TN-28							TRANSISTOR NETWORK	1	
6-31	N605, N607 N608, N610- N617			MEC TN-138B							TRANSISTOR NETWORK	11	
6-32	N609			MEC TN-130B							TRANSISTOR NETWORK	1	
6-33	N618			MEC TN-58							TRANSISTOR NETWORK	1	
6-34	P601			Cannon DD-50P							PLUG	1	
6-35	R601, R609 R614, R647 R648			MIL RC20GF223K							RESISTOR, Fixed composition, 22K $\pm 10\%$ 1/2W	5	
6-36	R602, R603 R612, R617 R620, R625 R627, R635			MIL RC20GF332K							RESISTOR, Fixed composition, 3300 $\Omega$ $\pm 10\%$ 1/2W	8	
6-37	R604, R621 R624, R631 R633, R638 R649, R650			MIL RC20GF102K							RESISTOR, Fixed composition, 100K $\pm 10\%$ 1/2W	8	
6-38	R605			MIL RC20GF471K							RESISTOR, Fixed composition, 470 $\Omega$ $\pm 10\%$ 1/2W	1	
6-39	R606			MIL RC20GF472K							RESISTOR, Fixed composition, 4700 $\Omega$ $\pm 10\%$ 1/2W	1	
6-40	R607, T611 R618, R622 R637, R641			MIL RC20GF473K							RESISTOR, Fixed composition, 47K $\pm 10\%$ 1/2W	6	
6-41	R608			MIL RC20GF152K							RESISTOR, Fixed composition, 1500 $\Omega$ $\pm 10\%$ 1/2W	1	
6-42	R610			Allen Bradley JLU-2531 or JA1L040S253UC							POTENTIOMETER, 25K 2W, Linear Taper	1	
6-43	R613, R626 R628, R629 R646			MIL RC20GF333K							RESISTOR, Fixed composition, 33K $\pm 10\%$ 1/2W	5	
6-44	R615, R636 R640			MIL RC20GF103K							RESISTOR, Fixed composition, 10K $\pm 10\%$ 1/2W	3	
6-45	R616, R623 R630, R643- R645			MIL RC20GF102K							RESISTOR, Fixed composition, 1000 $\Omega$ $\pm 10\%$ 1/2W	6	
6-46	R619			MIL RC20GF163J							RESISTOR, Fixed composition, 16K $\pm 5\%$ 1/2W	1	
6-47	R632			Allen Bradley JLU-5031 or JA1L040S503UC							POTENTIOMETER, 50K 2W, Linear Taper	1	

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
9-1				MEC 78-9A									
9-2	I901			Dialight Corp. 6S6								1	
9-3	P901			Cannon DD-50P								1	
9-4	S901			Centralab PA-2021								1	
9-5	XI901			Dialight Corp. 514001-113								1	
9-6				Whitso K-105								1	

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
6-48	R634			MIL RC20GF101K					RESISTOR, Fixed composition, 100Ω ±10% 1/2W			1	
6-49	R639			MIL RC20GF224K					RESISTOR, Fixed composition, 220K ±10% 1/2W			1	
6-50	R642			MIL RC20GF273K					RESISTOR, Fixed composition, 27K ±10% 1/2W			1	
6-51	R651			I. R. C. MDC					RESISTOR, Precision, 51.4K ±1% 1/2W			1	
6-52	R652			I. R. C. MDC					RESISTOR, Precision, 12K ±1% 1/2W			1	
6-53	R653			I. R. C. MDC					RESISTOR, Precision, 17K ±1% 1/2W			1	
6-54	R654			I. R. C. DCC					RESISTOR, Precision, 20K ±1% 1/2W			1	
6-55	R655			I. R. C. MDC					RESISTOR, Precision, 85K ±1% 1/2W			1	
6-56	S601			Centralab PA-2013					SWITCH, Rotary			1	
6-57	S602-S605			Micro 2PB11					SWITCH, Pushbutton			4	
6-58	S606			Carling 2GL63-73					SWITCH, Toggle, DPDT			1	
6-59	S607			Centralab PA-2003					SWITCH, Rotary			1	
6-60	TJ601			Cannon DD-50S					CONNECTOR			1	
6-61	MV601			Beede E-25					METER, 1.2 MA, (Scale 0-12) Horizontal			1	
6-62	XDS602			Eldema 11H4593					INDICATOR HOLDER			1	
6-63	XF601			Bussmann HKP					FUSE HOLDER			1	
6-64	XI601			Dialight Corp. 514001-111					INDICATOR HOLDER			1	
6-65	XM601- XM607			JAN TS103P02					SOCKET, 9 Pin, Mica filled			7	
6-66	XN601- XN618			JAN TS101P01					SOCKET, Octal, Mica filled			18	
6-67				Eldema 11H-4119					LENS CAP (Red)			1	
6-68				Whitso K-105					KNOB			2	



1	2	3	4	5	6	7	
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCURE-MENT CODE
					1 2 3 4 5 6 7		
9-1				MEC 76-9A	ASSEMBLY, POWER SUPPLY (-17V and -20V)	1	
9-2	C901- C905 C906			Mallory 20-71937	CAPACITOR, Computer Grade, 4000 $\mu$ f 60 vdc 2-1/16 x 4-1/2, Alum. can with Acetate Sleeve.	6	
9-3	C907			Cornell Dubilier PM4P5	CAPACITOR, Fixed, Mylar, .5 $\mu$ f 400 vdc	1	
9-4	C908			Mallory 20-71844	CAPACITOR, Computer Grade, 15,000 $\mu$ f 15 vdc 2-9/16 x 4-1/2 Alum. can with Acetate Sleeve	1	
9-5	CR901 CR902			G. E. ZJ50B(C60)	DIODE, 100 V	2	
9-6	CR903			Westinghouse IN1200	DIODE,	1	
9-7	CR904- CR907 CR909- CR911			G. E. IN1692	DIODE	7	
9-8	CR908			G. E. 4JA211BB1AC1	RECTIFIER	1	
9-9	L901			Sterling Trans. T3891	CHOKE	1	
9-10	N901			MEC TN-160	TRANSISTOR NETWORK	1	
9-11	Q901			Delco 2N443	TRANSISTOR, (Lug type Leads)	1	
9-12	R901			MIL RC20GF622J	RESISTOR, Fixed composition, 6.2K $\pm$ 5% 1/2W	1	
9-13	R902			Ohmite CLU-1521 or JA1L040S152UC	POTENTIOMETER, 1.5K 2W, Linear Taper	1	
9-14	R903			MIL RC20GF621J	RESISTOR, Fixed composition, 620 $\Omega$ $\pm$ 5% 1/2W	1	
9-15	R904			MIL RC20GF331K	RESISTOR, Fixed composition, 330 $\Omega$ $\pm$ 10% 1/2W	1	
9-16	R905			Ohmite 0600A	RESISTOR, Fixed, Wire wound, 5 $\Omega$ 100W (with Mounting Bracket #12)	1	
9-17	R906			MIL RC42GF332K	RESISTOR, Fixed composition, 3.3K $\pm$ 10% 2W	1	
9-18	R907- R909			Ward Leonard 20F1	RESISTOR, Fixed, Wire wound, 1 $\Omega$ 20W	3	
9-19	R910			MIL RC20GF101K	RESISTOR, Fixed composition, 100 $\Omega$ $\pm$ 10% 1/2W	1	
9-20	T901			Industrial Trans. MP-8610	TRANSFORMER	1	
9-21	T902			Sterling Trans. T-3890	TRANSFORMER	1	
9-22	T903			Chicago Trans. FMS-6	TRANSFORMER	1	
9-23	TJ901- TJ903			H. H. Smith 221	JACK, Midget Banana (Black)	3	
9-24	XN901			Amphenol 77-MIP-11T	SOCKET, 11 Pin	1	

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
1-1				MEC 78-1AAA	ASSEMBLY,				Connector		Bracket	1	
1-2	F1 F2			Bussmann Ban	FUSE,	20			amp			2	
1-3	F3			Bussman Ban	FUSE,	2			amp			1	
1-4	I1			Dialight 6S6-125V	LAMP,				Candelabra,		Clear	1	
1-5				Amphenol MS-3102A-404P	CONNECTOR,							3	
1-6	J16			Cannon MS3102A-18-13P MS3106B-18-13S MS3057-10A	CONNECTOR,				with mating connector and cable		clamp	1	
1-7	J15			Cannon MS 3102A-18-11P MS 3106B-18-11S MS 3057-10A	CONNECTOR,				with mating connector and cable		clamp	1	
1-8	S1			Cutler - Hammer ST52N	SWITCH,	125			v, 25 amp, DPDT			1	
1-9	XF1 - XF3			Bussmann Type HPC	FUSEHOLDER							3	
1-10				Dialight Corp. #514001-111	INDICATOR				HOLDER			1	
1-11				Allen-Bradley #702A0D92	CONTACTOR							1	

1	2	3	4	5	6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCUREMENT CODE
					1 2 3 4 5 6 7		
7-1				MEC 76-7A	ASSEMBLY 20-BIT SHIFT REGISTER	1	
7-2	C701			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000 $\mu$ f 500vdc $\pm$ 10%	1	
7-3	C702			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01 $\mu$ f 400 vdc	1	
7-4	C703			MIL CM-19B-471K	CAPACITOR, Fixed, Mica, 470 $\mu$ f 500 vdc $\pm$ 10%	1	
7-5	C704			Fansteel F110-1	CAPACITOR, (Blu-Cap) 10 $\mu$ f 25 vdc Insulated Case.	1	
7-6	C705 C707			Fansteel F308-1	CAPACITOR, (Blu-Cap) 100 $\mu$ f 30 vdc Insulated Case.	2	
7-7	C706			Cornell Dubilier PM4S5	CAPACITOR, Fixed Mylar, .05 $\mu$ f 400 vdc	1	
7-8	CR701- CR703			G. E. IN1692	DIODE	3	
7-9	CR704			Transitron T12G or Clevite CTP-503	DIODE	1	
7-10	DS701- DS720			MEC 16-102	INDICATOR	20	
7-11	M701- M720			MEC MN-11	CORE, Magnetic	20	
7-12	M721			MEC MN-13	CORE, Magnetic	1	
7-13	N701- N720			MEC TN-144	TRANSISTOR NETWORK	20	
7-14	N721			MEC TN-130B	TRANSISTOR NETWORK	1	
7-15	N722			MEC TN-58	TRANSISTOR NETWORK	1	
7-16	N723			MEC TN-138B	TRANSISTOR NETWORK	1	
7-17	P701			Cannon DD-50P	PLUG	1	
7-18	R701- R720			MIL RC20GF273K	RESISTOR, Fixed composition, 27K $\pm$ 10% 1/2W	20	
7-19	R721 R722			MIL RC20GF103K	RESISTOR, Fixed composition, 10K $\pm$ 10% 1/2W	2	
7-20	R723			MIL RC20GF182K	RESISTOR, Fixed composition, 1.8K $\pm$ 10% 1/2W	1	
7-21	R724			MIL RC20GF332K	RESISTOR, Fixed composition, 3.3K $\pm$ 10% 1/2W	1	
7-22	R725			MIL RC20GF163J	RESISTOR, Fixed composition, 16K $\pm$ 5% 1/2W	1	
7-23	R726 R728			MIL RC20GF102J	RESISTOR, Fixed composition, 1K $\pm$ 5% 1/2W	2	
7-24	R727			MIL RC20GF161J	RESISTOR, Fixed composition, 160 $\Omega$ $\pm$ 5% 1/2W	1	
7-25	TJ701			Cannon DD-50S	CONNECTOR	1	
7-26	XM701- XM721			JAN TS103P02	SOCKET, 9 Pin Miniature, Mica filled	21	

1	2	3	4	5							6	7			
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCURE-MENT CODE		
					1	2	3	4	5	6	7				
7-27	XN701-XN723			JAN TS101P01									SOCKET, Octal, Mica filled	23	
8-1				MEC 71-8A									ASSEMBLY, Data Line Amplifier	1	
8-2	C801 C803			Cornell Dubilier PM 4S1									CAPACITOR, Fixed Mylar, .01 $\mu$ f, 400 vdc	2	
8-3	C826 C827			Cornell Dubilier PM 4S2									CAPACITOR, Fixed Mylar, .02 $\mu$ f, 400 vdc	2	
8-4	C811- C814			Cornell Dubilier PM4P1									CAPACITOR, Fixed Mylar, .1 $\mu$ f, 400 vdc	4	
8-5	C802 C837			Cornell Dubilier PM6D5									CAPACITOR, Fixed Mylar, .005 $\mu$ f, 600 vdc	2	
8-6	C804 C805 C815			Cornell Dubilier PM2P47									CAPACITOR, Fixed Mylar, .47 $\mu$ f, 200 vdc	3	
8-7	C824			Cornell Dubilier PM4S5									CAPACITOR, Fixed Mylar, .05 $\mu$ f, 400 vdc	1	
8-8	C806			Mil CM-19B-501K									CAPACITOR, Fixed Mica, 500 $\mu$ f, 500 vdc $\pm 10\%$	1	
8-9	C807 C809 C810			Mil CM-19B-202K									CAPACITOR, Fixed Mica, 2000 $\mu$ f, 500 vdc $\pm 10\%$	3	

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCURE-MENT CODE
					1	2	3	4	5	6	7		
8-10	C817- C819 C821 C825 C828			Mil CM-19B-101K			CAPACITOR,	Fixed Mica, 100 $\mu$ f $\pm$ 10%, 500 vdc				6	
8-11	C816			Mil CM-19B-501K			CAPACITOR,	Fixed Mica, 500 $\mu$ f $\pm$ 10% 500 vdc				1	
8-12	C820			Mil CM-19B=152K			CAPACITOR,	Fixed Mica, 1500 $\mu$ f, $\pm$ 10% 500 vdc				1	
8-13	C829- C831			Mil CM-19B-560K			CAPACITOR,	Fixed Mica, 56 $\mu$ f, $\pm$ 10%, 500 vdc				3	
8-14	C808 C832 C833			Aerovox AEP8J			CAPACITOR,	Fixed 40 $\mu$ f, 450 v, Plug-in				3	
8-15	C834			Aerovox AEP88J			CAPACITOR,	Fixed, 40-40 $\mu$ f, 450 v, Dual Plug In				1	
8-16	C822			Mil CM-19B=102K			CAPACITOR,	Fixed Mica, 1000 $\mu$ f, $\pm$ 10% 500vdc				1	
8-17	C823			Mil CM-19B-471K			CAPACITOR,	Fixed Mica, 470 $\mu$ f, $\pm$ 10% 500 vdc				1	
8-18	C835			Mil CM-19B-470K			CAPACITOR,	Fixed Mica, 47 $\mu$ f, $\pm$ 10% 500 vdc				1	
8-19	CR801- CR804 CR809- CR815			Hughes HD6227			DIODE					11	
8-20	CR816- CR824			G. E. INI695			DIODE					9	
8-21	CR805- CR808			Pacific Semi-Conductor PC 030			DIODE					4	
8-22	F801			Bussmann AGC			FUSE,	1 amp				1	
8-23	DS801- DS804			Eldema ICG12-4535			LAMP,	Neon to Spec. 21C-3864-7				4	
8-24	L801 L802			UTC MQA-17			INDUCTOR,	10 hy, 7 ma. max.				2	
8-25	L803			UTC HVC-8			INDUCTOR					1	
8-26	P801			Cannon DD-50P			PLUG,	Male, 50 Pin contact, 5 amp. rating				1	
8-27	R802			Mil RC20GF434J			RESISTOR,	Fixed Composition, 430K, $\pm$ 5% 1/2 w				1	

1	2	3		4	5							6	7
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
8-28	R803 R809 R811 R820 R821			Mil RC20GF244J				RESISTOR,	Fixed composition, 240K, ±5% 1/2 w			5	
8-29	R805 R883 R823 R825 R826 R829 R831 R834- R837 R861 R866 R877 R880 R881 R854			Mil RC20GF104K				RESISTOR,	Fixed Composition, 100K, ±10% 1/2 w			17	
8-30	R806 R830 R859			Mil RC20GF563K				RESISTOR,	Fixed Composition, 56K, ±10%, 1/2 w			3	
8-31	R807 R862 R865			Mil RC20GF124K				RESISTOR,	Fixed composition, 120K, ±10% 1/2 w			3	
8-32	R815 R819			Mil RC20GF224K				RESISTOR,	Fixed composition, 220K, ±10% 1/2 w			2	
8-33	R816			Mil RC20GF102K				RESISTOR,	Fixed composition, 1K ±10% 1/2 w			1	
8-34	R817 R818 R833 R868 R869 R871			Mil RC20GF624J				RESISTOR,	Fixed composition, 62K ±5% 1/2 w			6	
8-35	R828 R839 R845 R851			Mil RC20GF204J				RESISTOR,	Fixed composition, 200K, ±5% 1/2 w			4	
8-36	R832 R838 R844 R850 R863 R864 R867 R870 R872			Mil RC20GF624J				RESISTOR,	Fixed composition, 620 K ±5% 1/2 w			9	
8-37	R855			Mil RC20GF824K				RESISTOR,	Fixed composition, 820K ±10% 1/2 w			1	

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
8-38	R857			Mil RC20GF333K			RESISTOR,	Fixed composition,	33K ±10%,	1/2 w	1		
8-39	R810			Mil RC20GF202J			RESISTOR,	Fixed composition	2K, ±5%	1/2 w	1		
8-40	R808 R856 R858			Mil RC20GF105K			RESISTOR,	Fixed composition,	1M ±10%	1/2 w	3		
8-41	R824 R827			Mil RC20GF124K			RESISTOR,	Fixed composition,	1.2M, ±10%	1/2 w	2		
8-42	R860			Mil RC20GF222K			RESISTOR,	Fixed composition,	2.2K, ±10%	1/2 w	1		
8-43	R814			Mil RC42GF222K			RESISTOR,	Fixed composition,	2.2K, ±10%	2 w	1		
8-44	R840 R841 R846 R847 R852 R853			Mil RC42GF433J			RESISTOR,	Fixed composition,	43K, ±5%,	2 w	6		
8-45	R842			Mil RC20GF205J			RESISTOR,	Fixed composition,	2M, ±5%	1/2 w	1		
8-46	R873 R874			Mil RC42GF101K			RESISTOR,	Fixed composition	100Ω ±10%	2W	2		
8-47	R879			Mil RC42GF511J			RESISTOR,	Fixed composition,	510Ω ±5%	2 w	1		
8-48	R875			Ward Leonard 10F8000			RESISTOR,	Fixed, wire wound	8K, 10w		1		
8-49	R878			Ward Leonard 10F3000			RESISTOR,	Fixed, wire wound	3K, 10w		1		
8-50	R876			Mil RC42GF202J			RESISTOR,	Fixed composition,	2K, ±5%,	2 w	1		
8-51	R849 R843			Allen Bradley JAIL 040S255UC			POTENTIOMETER,	2.5M 2w, Linear	Taper		2		
8-52	R822			Allen Bradley JAIL040S503UC			POTENTIOMETER,	50K, 2w, Linear	Taper		1		
8-53	R801			Allen Bradley JAIL040SI04UC			POTENTIOMETER,	100K, 2W Linear	taper		1		
8-54	R804			Mil RC20GF271K			RESISTOR,	Fixed Composition	270Ω ±10%	1/2 w	1		
8-55	R812			Mil RC20GF432K			RESISTOR,	Fixed composition,	4.3K, ±10%	1/2 w	1		
8-56	R813			Mil RC20GF473K			RESISTOR,	Fixed composition,	47K, ±10%	1/2 w	1		
8-57	R848			Mil RC20GF105J			RESISTOR,	Fixed composition,	1M, ±5%	1/2 w	1		
8-58	R882			Mil RC20GF433K			RESISTOR,	Fixed composition,	43K, ±10%	1/2 w	1		

1	2	3	4	5							6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
8-59	T801			Triad JO-13					TRANSFORMER			1	
8-60	T802			Chicago Std. PHC-60					TRANSFORMER			1	
8-61	TJ801			Cannon					CONNECTOR, Female, 50 Pin Contact, 5 amp rating			1	
8-62	V801			Comm. 6660					TUBE, Electron			1	
8-63	V802 V803 V805- V807			Comm. 5963					TUBE, Electron			5	
8-64	V804 V808- V811			Comm 12AT7					TUBE, Electron			5	
8-65	V812 V815			Comm. OB2					TUBE, Electron, voltage regulator			2	
8-66	V813 V814			Comm. OA2					TUBE, Electron, Voltage Regulator			2	
8-67	XC808 XC832 XC833			Jan TS101PO1					SOCKET, Octal, mica filled			3	
8-68	XDS801- XDS804			Eldema 11H4593					INDICATOR holder			4	
8-69	XF801			Bussmann HKP					FUSE holder			1	
8-70	XV802- XV811			Jan TS103PO1					SOCKET, 9 Pin Miniature, Mica Filled			10	
8-71	XV801 XV812- XV815			Jan TS102PO1					SOCKET, 7 Pin miniature, Mica Filled			5	
8-72				Jan TS102U02					SHIELD, Tube			1	
8-73				Jan TS102U03					SHIELD, Tube			4	
8-74				Jan TS103U02					SHIELD, Tube			10	
8-75				Eldema 11H-4110					LENS Cap (Translucent)			3	
8-76				Eldema 11H-4119					LENS Cap (Red)			1	



1	2	3		4	5							6	7
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
1				McLean 2EB508C			ASSEMBLY			BLOWER		1	

1	2	3	4	5	6	7	
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION	UNIT PER ASSY.	PROCUREMENT CODE
					1 2 3 4 5 6 7		
4-1				MEC 165-4C	ASSEMBLY, POWER SUPPLY	1	
4-2	C401 C402 C421-C423			Mallory 20-71937	CAPACITOR, Computer Grade, 4000 $\mu$ f 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	5	
4-3	C403 C425 C443 C444			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01 $\mu$ f 400 vdc	4	
4-4	C424			Cornell Dubilier PM4P1	CAPACITOR, Fixed, Mylar, .1 $\mu$ f 400 vdc	1	
4-5	C404 C426			Fansteel F308-1	CAPACITOR, Blu-cap, 100 $\mu$ f 30 vdc	2	
4-6	C441 C442			Mallory 20-71855	CAPACITOR, Computer Grade, 2000 $\mu$ f 100 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	2	
4-7	C445			Fansteel F316-1	CAPACITOR, Blu-cap, 30 $\mu$ f 100 vdc	1	
4-8	CR401 CR421			G. E. 4JA211AB1AC2	RECTIFIER	3	
4-9	CR402 CR422			International Rectifier IN1519	DIODE, Zener (1Z4.7)	2	
4-10	CR442			International Rectifier IN1524	DIODE, Zener (1Z12)	1	
4-11	F401 F403			Bussmann AGC	FUSE, 1 Amp	2	
4-12	F402			Bussmann AGC	FUSE, 3 Amp	1	
4-13	F404			Bussmann MDX	FUSE, Fusetron, Slo-Blow, 3 Amp.	1	
4-14	P401			Cannon DD-50P	PLUG	1	
4-15	Q423 Q442			Delco 2N553	TRANSISTOR, (Mount with Parts #100 & #101)	2	
4-16	Q401 Q421 Q441 Q422			Delco 2N443	TRANSISTOR, (Lug type Leads)	4	
4-17	Q402 Q403 Q424 Q443			G. E. 2N525	TRANSISTOR	4	
4-18	Q404 Q425 Q444			Sylvania 2N377A	TRANSISTOR	3	
4-19	R401, R402 R421A R421B R441 R442			Ward Leonard 5X1	RESISTOR, Axiohm, 1 $\Omega$ 5W	6	
4-20	R403 R443			Ward Leonard 5X2	RESISTOR, Axiohm, 2 $\Omega$ 5W	2	
4-21	R404 R425 R444			MIL RC42GF102K	RESISTOR, Fixed composition, 1K $\pm$ 10% 2W	3	

1	2	3	4	5							6	7
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	1	2	3	4	5	6	7	7
											UNIT PER ASSY.	PROCUREMENT CODE
4-22	R405			MIL RC42GF151K					RESISTOR, Fixed composition, 150Ω ±10% 2W		1	
4-23	R406			MIL RC20GF681K					RESISTOR, Fixed composition, 680Ω ±10% 1/2W		1	
4-24	R407 R428 R447			MIL RC20GF101K					RESISTOR, Fixed composition, 100Ω ±10% 1/2W		3	
4-25	R408			MIL RC20GF122K					RESISTOR, Fixed composition, 1.2K ±10% 1/2W		1	
4-26	R409 R430 R449			MIL RC20GF822K					RESISTOR, Fixed composition, 8.2K ±10% 1/2W		3	
4-27	R410 R431 R450			MIL RC20GF621J					RESISTOR, Fixed composition, 620Ω ±5% 1/2W		3	
4-28	R411 R432			MIL RC20GF472K					RESISTOR, Fixed composition, 4.7K ±10% 1/2W		2	
4-29	R412			MIL RC32GF121K					RESISTOR, Fixed composition, 120Ω ±10% 1W		1	
4-30	R414 R435			Chicago Tel. RA20LASB250A					POTENTIOMETER, 25Ω 2W		2	
4-31	R415			MIL RC32GF820J					RESISTOR, Fixed composition, 82Ω ±5% 1W		1	
4-32	R413			MIL RC42GF131J					RESISTOR, Fixed composition, 130Ω ±5% 2W		1	
4-33	R422			Ward Leonard 10F1					RESISTOR, Fixed, Wire wound, 1Ω 10W		1	
4-34	R423 R424			Ward Leonard 10F2					RESISTOR, Fixed, Wire wound, 2Ω 10W		2	
4-35	R426 R437			Ward Leonard 10F150					RESISTOR, Fixed, Wire wound, 150Ω 10W		2	
4-36	R427 R446			MIL RC32GF681K					RESISTOR, Fixed composition, 680Ω ±10% 1W		2	
4-37	R429 R448			MIL RC32GF122K					RESISTOR, Fixed composition, 1.2K ±10% 1W		2	
4-38	R433 R416			MIL RC42GF271K					RESISTOR, Fixed composition, 270Ω ±10% 2W		2	
4-39	R436			MIL RC32GF510J					RESISTOR, Fixed composition, 51Ω ±5% 1W		1	
4-40	R434			MIL RC42GF181J					RESISTOR, Fixed composition, 180Ω ±5% 2W		1	
4-41	R451			MIL RC42GF302J					RESISTOR, Fixed composition, 3K ±5% 2W		1	
4-42	R453			Allen Bradley JLU-1011 or JA1L040S101UC					POTENTIOMETER, 100Ω 2W, Linear Taper		1	
4-43	R454			MIL RC42GF272J					RESISTOR, Fixed composition, 2.7K ±5% 2W		1	
4-44	R455			Ward Leonard 5X500					RESISTOR, Fixed, Axiohm, 500Ω 5W		1	
4-45	R452			MIL RC32GF561J					RESISTOR, Fixed composition, 560Ω ±5% 1W		1	
4-46	R445			Ward Leonard 10F250					RESISTOR, Fixed, Wire wound, 250Ω 10W		1	
4-47	T401			TTI 5486					TRANSFORMER		1	

1	2	3		4	5							6	7
ITEM NO.	REFER. DESIGNATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION							UNIT PER ASSY.	PROCUREMENT CODE
					1	2	3	4	5	6	7		
4-48	TJ401-TJ404			H. H. Smith 221				JACK, Midget		Banana (Black)		4	
4-49	XF401-XF404			Bussmann HKP				FUSEHOLDER				4	

## **CHAPTER VIII**

### **WIRE LIST**

INDEX					
WIRE NO.	REFERENCE TERMINAL	PAGE DESIGNATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
J1		3-4	◇	SR #1	
J2		5-7		SR #2	
J3		8-10		SR #3	
J4		11-13		SR #4	
J5		14-15		SR #5	
J6		16-18		SR #6	
J7		19-21		SR #7	
J9		22-25		Control	
J11		26-28		Data Line Amp	
J13		29-31		Power Supply	
J14		32-33		Power Supply	
J15		34		Power Connector	
J16		35		Signal Input	
J115		36-38		Signal Output	
J116		39-41		Signal Output	
J117		42-44		Signal Output	
-85V		45		-85 Volt Bus	
-20V		46		-20 Volt Bus	
+12V		47		+12 Volt Bus	
0V		48		0 Volt Bus	
I1		49		Power Indicator	
F1		50		F1 Fuse	
F3		51		F3 Fuse	
F2		52		F2 Fuse	
NOTES:					

INDEX					
WIRE NO.	REFERENCE TERMINAL	PAGE DESIGNATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	SW1	53	◇	Switch	
	Blower	54		Blower	
	TB2	55		TB2	
	K1	56		K1	
	J12	57-58		Recorder Control	
	J17	59		Recorder Input Connector	
	J18	60		Recorder Output Connector	
NOTES:					

J1 SHIFT REGISTER #1					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J117-1	1	Output F/F #1	22 W-V
	2	J117-A	1	Output F/F #2	22 W-BL
	3	J117-2	1	Output F/F #3	22 W-G
	4	J117-B	1	Output F/F #4	22 W-Y
	5	J117-3	1	Output F/F #5	22 W-O
	6	J117-C	1	Output F/F #6	22 V
	7	J117-4	1	Output F/F #7	22 8L
	8	J117-D	1	Output F/F #8	22 W-O
	9	J117-5	1	Output F/F #9	22 Y
	10	J117-E	1	Output F/F #10	22 O
	11	J116-16	1	Output F/F #11	22 W-V
	12	J116-P	1	Output F/F #12	22 W-BL
	13	J116-17	1	Output F/F #13	22 W-G
	14	J116-Q	1	Output F/F #14	22 W-Y
	15	J116-18	1	Output F/F #15	22 W-O
	16	J116-R	1	Output F/F #16	22 V
	17	J116-19	1	Output F/F #17	22 BL
	18	J116-S	1	Output F/F #18	22 G
	19	J116-20	1	Output F/F #19	22 Y
	20	J116-T	1	Output F/F #20	22 O
	21				
	22				
	23				
	24				
	25				
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A 78NL1A	SHEET 3 OF SHEET

J1 SHIFT REGISTER #1					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34	J2-34	1	Core Shift	22 Y
	35				
	36	J2-36	1	F/F Reset Trigger	22 O
	37				
	38	J2-38	1	Read Gate	22 G
	39				
	40	J2-41	1	Core Output	22 W/BR
	41	J9-14	1	Core Input	22 BR
	42	J14-17V-3		-17V	20 W/S
	43	J14-17V-3		-17V	20 W/S
	44	+12V Bus#1		+12V	20 R
	45	J14-0V-3		0V	20 BK
	46	J14-0V-3		0V	20 BK
	47	J14-20V-3		-20V	20 S
	48			-20V	
	49	-85VBus#1		-85V	22 W/BK
	50	Frame		Chassis Ground	
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A 78NL1A	SHEET 4 OF SHEETS

J2 SHIFT REGISTER #2					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
1		J116-11	1	Output F/F #1	22 W-V
2		J116-K	1	Output F/F #2	22 W-BL
3		J116-12	1	Output F/F #3	22 W-G
4		J116-L	1	Output F/F #4	22 W-Y
5		J116-13	1	Output F/F #5	22 W-O
6		J116-M	1	Output F/F #6	22 V
7		J116-14	1	Output F/F #7	22 BL
8		J116-N	1	Output F/F #8	22 G
9		J116-15	1	Output F/F #9	22 W-V
10		J116-O	1	Output F/F #10	22 W-BL
11		J115-21	1	Output F/F #11	22 W-G
12		J115 U	1	Output F/F #12	22 W-Y
13		J115-22	1	Output F/F #13	22 W-O
14		J115-V	1	Output F/F #14	22 V
15		J115-23	1	Output F/F #15	22 BL
16		J115-W	1	Output F/F #16	22 G
17		J115-24	1	Output F/F #17	22 Y
18		J115-X	1	Output F/F #18	22 O
19		J115-25	1	Output F/F #19	22 W-V
20		J115-Y	1	Output F/F #20	22 W-BL
21					
22					
23					
24					
25					
NOTES:					

J2 SHIFT REGISTER #2					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34	J1-34	1	Core Shift	22 Y
	34	J3-34	1	Core Shift	22 Y
	35				
	36	J1-36	1	F/F Reset Trigger	22 O
	36	J3-36	1	F/F Reset Trigger	22 O
	37				
	38	J1-38	1	Read Gate	22 G
	38	J3-38	1	Read Gate	22 G
	39				
	40	J3-41	1	Core Output	22 BR
	41	J2-40	1	Core Input	22 W/BR
	42	J14-17V-4	2	-17V	20 W/S
	43	J14-17V-4	2	-17V	20 W/S
	44	+12VBus-2	2	+12V	20 R
	45	J14-0V-4	2	0V	20 BK
	46	J14-0V-4	2	0V	20 BK
	47	J14-20V-4	2	-20V	20 S
NOTES:					



J2 SHIFT REGISTER #2					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	48			-20V	
	49	-85VBus-2		-85V	22 W/BK
	50	Frame		Chassis Ground	20 BK
NOTES:					

J3 SHIFT REGISTER #3					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J115-11	1	Output F/F #1	22 W-G
	2	J115-K	1	Output F/F #2	22 W-Y
	3	J115-12	1	Output F/F #3	22 W-O
	4	J115-L	1	Output F/F #4	22 V
	5	J115-13	1	Output F/F #5	22 BL
	6	J115-M	1	Output F/F #6	22 G
	7	J115-14	1	Output F/F #7	22 Y
	8	J115-N	1	Output F/F #8	22 O
	9	J115-15	1	Output F/F #9	22 W-V
	10	J115-0	1	Output F/F #10	22 W-BL
	11	J115-16	1	Output F/F #11	22 W-G
	12	J115-P	1	Output F/F #12	22 W-Y
	13	J115-17	1	Output F/F #13	22 W-O
	14	J115-Q	1	Output F/F #14	22 V
	15	J115-18	1	Output F/f #15	22 BL
	16	J115-R	1	Output F/F #16	22 G
	17	J115-19	1	Output F/F #17	22 Y
	18	J115-S	1	Output F/F #18	22 O
	19	J115-20	1	Output F/F #19	22 O
	20	J115-T	1	Output F/F #20	22 W-V
	21				
	22				
	23				
	24				
	25				
NOTES:					

J3 Shift Register #3					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34	J2-34	1-	Core Shift	22 Y
	34	J4-34	1	Core Shift	22 Y
	35				
	36	J4-36	1	F/F Reset Trigger	22 0
	36	J2-36	1	F/F Reset Trigger	22 0
	37				
	38	J2-38	1	Read Gate	22 G
	38	J4-38	1	Read Gate	22 G
	39				
	40	J4-41	1	Core Output	22 W/BR
	41	J3-40	1	Core Input	22 BR
	42	J14-17V-5	2	-17V	20 W/S
	43	J14-17-5	2	-17V	20 W/S
	44	+12VBUS-3	2	+12V	20 R
	45	J140V-5	2	0V	20 BK
	46	J140V-5	2	0V	20 BK
	47	J14-20V-5	2	-20V	20 S
	48			-20V	
NOTES:					

J3 Shift Register #3					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	49	-85VBUS-3	2	-85V	22 W/BK
	50	Frame		Chassis Ground	20 BK
NOTES:					

J4

## SHIFT REGISTER #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
1	J117-F	1	Output F/F #1	68	22	W-BL
2	J117-7	1	Output F/F #2	67	22	W-G
3	J117-6	1	Output F/F #3	66	22	W-Y
4	J117-8	1	Output F/F #4	65	22	W-O
5	J117-H	1	Output F/F #5	64	22	V
6	J117-9	1	Output F/F #6	63	22	BL
7	J117-I	1	Output F/F #7	62	22	G
8	J117-10	1	Output F/F #8	61	22	Y
9	J117-J	1	Output F/F #9	60	22	W-V
10	J117-11	1	Output F/F #10	59	22	W-BL
11	J116-1	1	Output F/F #11	58	22	W-G
12	J116-A	1	Output F/F #12	57	22	W-Y
13	J116-2	1	Output F/F #13	56	22	W-O
14	J116-B	1	Output F/F #14	55	22	V
15	J116-3	1	Output F/F #15	54	22	BL
16	J116-C	1	Output F/F #16	53	22	GR
17	J116-4	1	Output F/F #17	52	22	Y
18	J116-D	1	Output F/F #18	51	22	O
19	J116-5	1	Output F/F #19	50	22	W-G
20	J116-E	1	Output F/F #20	49	22	W-BL
21						
22						
23						
24						
25						

NOTES:

J4

## Shift Register #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
26						
27						
28						
29						
30						
31						
32						
33						
34		J3-34	1	Core Shift	22	Y
34		J9-12	1	Core Shift	22	Y
35						
36		J3-36	1	F/F Reset Trigger	22	O
36		J9-7	1	F/F Reset Trigger	22	O
37						
38		J3-38	1	Read Gate	22	G
38		J9-6	1	Read Gate	22	G
39						
40		J5-41	1	Core Output	22	BR
41		J3-40	1	Core Input	22	W/BR
42		J14-17V-6	2	-17V	20	W/S
43		J14-17V-6	2	-17V	20	W/S
44		+12VBUS-4	2	+12V	20	R
45		J14-OV-6	2	OV	20	BK
46		J14-OV-6	2	OV	20	BK
47		J14-20V-6	2	-20V	20	S
48				-20V		

NOTES:

J4 Shift Register #4					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE
	49	-85VBUS-4	2	-85V	22
	50	Frame		Chassis Ground	20
					W/BK
					BK

NOTES:

J5 Shift Register #5					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE
	1	J115-6	1	Output F/F #1 Bit #48	22
	2	J115-F	1	Output F/F #2 Bit #47	22
	3	J115-7	1	Output F/F #3 Bit #46	22
	4	J115-6	1	Output F/F #4 Bit #45	22
	5	J115-8	1	Output F/F #5 Bit #44	22
	6	J115-H	1	Output F/F #6 Bit #43	22
	7	J115-9	1	Output F/F #7 Bit #42	22
	8	J115-I	1	Output F/F #8 Bit #41	22
	9	J115-10	1	Output F/F #9 Bit #40	22
	10	J115-J	1	Output F/F #10 Bit #39	22
	11	J115-1	1	Output F/F #11 Bit #38	22
	12	J115-A	1	Output F/F #12 Bit #37	22
	13	J115-2	1	Output F/F #13 Bit #36	22
	14	J115-B	1	Output F/F #14 Bit #35	22
	15	J115-3	1	Output F/F #15 Bit #34	22
	16	J115-C	1	Output F/F #16 Bit #33	22
	17	J115-4	1	Output F/F #17 Bit #32	22
	18	J115-D	1	Output F/F #18 Bit #31	22
	19	J115-5	1	Output F/F #19 Bit #30	22
	20	J115-E	1	Output F/F #20 Bit #29	22
	21				W/G
	22				W/Y
	23				W/O
	24				V
	25				BL
					G
					Y
					O
					W/V
					W/BL

NOTES:

J5 SHIFT REGISTER #5					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34	J6-34		Core Shift	22 Y
	35				
	36	J6-36	1	F/F Reset Trigger	22 0
	37				
	38	J6-38		Read Gate	22 G
	39				
	40	J6-41	1	Core Output	22 W/BK
	41	J4-40	1	Core Input	22 BR
	42	J14-17V-7	2	-17V	20 W/S
	43	J14-17V-7	2	-17V	20 W/S
	44	+12VBus-5	2	+12V	20 R
	45	J14-0V-7	2	0V	20 BK
	46	J14-0V-7	2	0V	20 BK
	47	J14-20-7	2	-20V	20 S
	48			-20V	
	49	-85VBus-5	2	-85V	22 W/BK
	50	Frame		Chassis Ground	
NOTES:					

J6 SHIFT REGISTER #6					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
	1	J117-12	1	Output F/F #1 Bit	22 W-G
	2	J117-L	1	Output F/F #2 Bit	22 W-Y
	3	J117-13	1	Output F/F #3 Bit	22 W-O
	4	J117-M	1	Output F/F #4 Bit	22 V
	5	J117-14	1	Output F/F #5 Bit	22 BL
	6	J117-N	1	Output F/F #6 Bit	22 G
	7	J117-15	1	Output F/F #7 Bit	22 Y
	8	J117-0	1	Output F/F #8 Bit	22 0
	9	J117-16	1	Output F/F #9 Bit	22 W-V
	10	J117-P	1	Output F/F #10 Bit	22 W-BL
	11	J117-17	1	Output F/F #11 Bit	22 W-G
	12	J117-Q	1	Output F/F #12 Bit	22 W-Y
	13	J117-18	1	Output F/F #13 Bit	22 W-O
	14	J117-R	1	Output F/F #14 Bit	22 V
	15	J117-19	1	Output F/F #15 Bit	22 BL
	16	J117-S	1	Output F/F #16 Bit	22 G
	17	J117-20	1	Output F/F #17 Bit	22 Y
	18	J117-T	1	Output F/F #18 Bit	22 0
	19	J117-21	1	Output F/F #19 Bit	22 W-V
	20	J117-U	1	Output F/F #20 Bit	22 W-BL
	21				
	22				
	23				
	24				
	25				
NOTES:					





J7 SHIFT REGISTER #7					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	48			-20V	
	49	-85V-7	2	-85V	22 W/BR
	50	Frame		Chassis Ground	20 BK

NOTES:

J9 CONTROL					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J11-13	1	Data	Coax
	2				
	3	J11-7	1	1KC	22 Y
	4				
	5	J11-9	1	Detected EOW	Coax
	6	J4-38	1	Gate Driver	22 G
	6	J7-38	1	Gate Driver	22 G
	7	J4-36	1	F/F Reset Trigger	22 0
	7	J7-36	1	F/F Reset Trigger	22 0
	8				
	9				
	10				
	11				
	12	J4-34	1	CD Trigger	22 Y
	12	J7-34	1	CD Trigger	22 Y
	13				
	14	J1-41	1	To 20 Core SR	22 BR
	15				
	16	J117-6	1	To D/A Hold Relays	22 W/BR
	17				
	18				
	19				
	20				
	21				
	22				

NOTES:





J9 CONTROL					WIRE LIST	
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	41					
	42					
	43					
	44					
	45					
	46					
	47					
	48					
NOTES:						
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA						
					A 78WLL1A SHEET 25 OF SHEETS	

J11 DATA LINE AMPLIFIER							WIRE LIST	
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR		
	1							
	2							
	3							
	4							
	5							
	6							
	7	J9-3	1	1KC OUT	22	Y		
	8							
	9	J9-5	1	EQW OUT	Coax			
	10							
	11			SOW OUT				
	12							
	13	J9-1	1	Data Out	Coax			
	14							
	15	J12-5	1	Data In	Coax			
	16							
	17	J12-7	1	Data In	Coax			
	18							
	19							
	20							
	21							
	22							
	23							
	24							
	25							
NOTES:								
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA								
					A 78WLL1A SHEET 26 OF SHEETS			

J-11 DATA LINE AMPLIFIER					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
26					
27					
28					
29					
30					
31					
32					
33					
34		K1-6	2	120VAC Ø1 Switched	18 W/S
35				120VAC Ø1 Switched	
36		TB2-6	2	120VAC Common	18 W
37					
38					
39					
40					
41					
42					
43					
44					
45		OV-3		OV	20 BK
46		OV-4		OV	20 BK
47					
48					
49		J17-1	1	Recorder Input	Coax
50					
NOTES:					
				MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA	
				WIRE LIST	A 78WLLA SHEET 27 OF SHEETS

J-11 DATA LINE AMPLIFIER					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	34---				
	35---				
	36---				
	37---				
	45---				
	46---				
NOTES:					
				MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA	
				WIRE LIST	A 78WLLA SHEET 28 OF SHEETS

J13 Power Supply					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	TB2-6	2	120VAC Common	18 W
	2				
	3				
	4	K1-6	2	120VACØ1 Switched	18 W/S
	5				
	6				
	7				
	8				
	9				
	10				
	11				
	12				
	13				
	14				
	15				
	16				
	17				
	18				
	19				
	20				
	21				
	22				
	23				
	24				
	25				

NOTES:

J13 Power Supply					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34		2	+12V Unregulated Output	
	35		2	-20V Unregulated Output	
	36				
	37				
	38				
	39				
	40				
	41				
	42				
	43				
	44	+12V-13	2	+12V	18 R
	45	OV-13	2	OV	20 BK
	46	OV-14	2	OV	20 BK
	47	-20V-1	2	-20V	20 S
	48	-20V-2	2	-20V	20 S
	49	-85V-8	2	-85V-8	20 W/BK
	50	Frame		Chassis Ground	

NOTES:

J13 Power Supply					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1				
	2				
	4				
	5				
	45				
	46				
	47				
	48				
NOTES:					

J14 POWER SUPPLY (-17V,-20V)					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	T903-1	K1-5	2	120VAC Ø1 Switched	#12 W/S
	T903-2	TB2-5	2	120VAC Common	#12 W
	OV-3	J1-45	2	SR #1	#20 BK
	OV-3	J1-46	2	SR #1	#20 BK
	OV-4	J2-45	2	SR #2	#20 BK
	OV-4	J2-46	2	SR #2	#20 BK
	OV-5	J3-45	2	SR #3	#20 BK
	OV-5	J3-46	2	SR #3	#20 BK
	OV-6	J4-45	2	SR #4	#20 BK
	OV-6	J4-46	2	SR #4	#20 BK
	OV-7	J5-45	2	SR #5	#20 BK
	OV-7	J5-46	2	SR #5	#20 BK
	OV-8	J6-45	2	SR #6	#20 BK
	OV-8	J6-46	2	SR #6	#20 BK
	OV-9	J7-45	2	SR #7	#20 BK
	OV-9	J7-46	2	SR #7	#20 BK
	OV-10	OV-1	2	OV	#18 BK
	OV-11	OV-2	2	OV	#18 BK
	-17V-3	J1-42	2	SR #1	#20 W/S
	-17V-3	J1-43	2	SR #1	#20 W/S
	-17V-4	J2-42	2	SR #2	#20 W/S
	-17V-4	J2-43	2	SR #2	#20 W/S
	-17V-5	J3-42	2	SR #3	#20 W/S
	-17V-5	J3-43	2	SR #3	#20 W/S
	-17V-6	J4-42	2	SR #4	#20 W/S
	-17V-6	J4-43	2	SR #4	#20 W/S
	-17V-7	J5-42	2	SR #5	#20 W/S
	-17V-7	J5-43	2	SR #5	#20 W/S
	-17V-8	J6-42	2	SR #6	#20 W/S
	-17V-8	J6-43	2	SR #6	#20 W/S
NOTES:					

J15 POWER CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	A	Sw1-1	2	120VAC (Hot)	12 S
	B	F2-1	2	120VAC Common	12 W
	C				
	D				
	E	Frame		Frame Ground	12 BK
NOTES: MS3102A-18-1					

J14 POWER SUPPLY (-17V, -20V)					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	-17V-9	J7-42	2	SR #7	#20 W/S
	-17V-9	J7-43	2	SR #7	#20 W/S
	-17V-10	J9-40	2	Control (Monitor	#22 W/S
	-17V-11	F3-1	2	-17V	#20 W/S
	-17V-12				
	-20V-3	J1-47	2	SR #1	#20 S
	-20V-4	J2-47	2	SR #2	#20 S
	-20V-5	J3-47	2	SR #3	#20 S
	-20V-6	J4-47	2	SR #4	#20 S
	-20V-7	J5-47	2	SR #5	#20 S
	-20V-8	J6-47	2	SR #6	#20 S
	-20V-9	J7-47	2	SR #7	#20 S
	-20V-10	J9-47	2	Control	#20 S
	-20V-11				
	-20V-12				
NOTES:					



J14 POWER SUPPLY (-17V, -20V)							J15 POWER CONNECTOR		
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR	TERMINAL	DESTINATION	CABLE
	-17V-9	J7-42	2	SR #7	#20	W/S	A	Sw1-1	2
	-17V-9	J7-43	2	SR #7	#20	W/S	B	F2-1	2
	-17V-10	J9-40	2	Control (Monitor)	#22	W/S	C		
	-17V-11	F3-1	2	-17V	#20	W/S	D		
	-17V-12						E	Frame	
	-20V-3	J1-47	2	SR #1	#20	S			
	-20V-4	J2-47	2	SR #2	#20	S			
	-20V-5	J3-47	2	SR #3	#20	S			
	-20V-6	J4-47	2	SR #4	#20	S			
	-20V-7	J5-47	2	SR #5	#20	S			
	-20V-8	J6-47	2	SR #6	#20	S			
	-20V-9	J7-47	2	SR #7	#20	S			
	-20V-10	J9-47	2	Control	#20	S			
	-20V-11								
	-20V-12								
NOTES:							NOTES: MS3102A-18--		
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA							MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA		
WIRE LIST							WIRE LIST		
SHEET 33 OF 34							SHEET 34 OF 34		

J14 POWER SUPPLY (-17V, -20V)							J15 POWER CONNECTOR		
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR	TERMINAL	DESTINATION	CABLE
	-17V-9	J7-42	2	SR #7	#20	W/S	A	Sw1-1	2
	-17V-9	J7-43	2	SR #7	#20	W/S	B	F2-1	2
	-17V-10	J9-40	2	Control (Monitor)	#22	W/S	C		
	-17V-11	F3-1	2	-17V	#20	W/S	D		
	-17V-12						E	Frame	
	-20V-3	J1-47	2	SR #1	#20	S			
	-20V-4	J2-47	2	SR #2	#20	S			
	-20V-5	J3-47	2	SR #3	#20	S			
	-20V-6	J4-47	2	SR #4	#20	S			
	-20V-7	J5-47	2	SR #5	#20	S			
	-20V-8	J6-47	2	SR #6	#20	S			
	-20V-9	J7-47	2	SR #7	#20	S			
	-20V-10	J9-47	2	Control	#20	S			
	-20V-11								
	-20V-12								
NOTES:							NOTES: MS3102A-18--		
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA							MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA		
WIRE LIST							WIRE LIST		
SHEET 33 OF 34							SHEET 34 OF 34		



J115						
SIGNAL CONNECTOR						
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-11	1	Bit #38	22	W-G
	A	J5-12	1	Bit #37	22	W-Y
	2	J5-13	1	Bit #36	22	W-O
	B	J5-14	1	Bit #35	22	V
	3	J5-15	1	Bit #34	22	BL
	C	J5-16	1	Bit #33	22	G
	4	J5-17	1	Bit #32	22	Y
	D	J5-18	1	Bit #31	22	O
	5	J5-19	1	Bit #30	22	W-V
	E	J5-20	1	Bit #29	22	W-BL
	6	J5-1	1	Bit #48	22	W-G
	F	J5-2	1	Bit #47	22	W-Y
	7	J5-3	1	Bit #46	22	W-O
	G	J5-4	1	Bit #45	22	V
	8	J5-5	1	Bit #44	22	BL
	H	J5-6	1	Bit #43	22	G
	9	J5-7	1	Bit #42	22	Y
	I	J5-8	1	Bit #41	22	O
	10	J5-9	1	Bit #40	22	W-V
	J	J5-10	1	Bit #39	22	W-BL
	11	J3-1	1	Bit #88	22	W-G
	K	J3-2	1	Bit #87	22	W-Y
	12	J3-3	1	Bit #86	22	W-O
	L	J3-4	1	Bit #85	22	V
	13	J3-5	1	Bit #84	22	BL
NOTES: MS-3102A-36-404P				MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA		
				WIRE LIST		
				A 78WL1A SHEET 36 OF 36		

J16 SIGNAL INPUT						
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	OV-15	1	Shields	20	BK
	B	J12-1	1	B-GE Input Line	Coax	
	C	J12-3	1	B-GE Input Line	Coax	
	D					

J116 SIGNAL CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	23	J7-19	1	Spare	22 V
	W	J7-20	1	Spare	22 W/O
	24			Spare	
	X			Spare	
	25			Spare	
	Y			Spare	
	+4.5	0VoltBus-9	2	0 Volts	20 BK
	-4.5	0VoltBus-10	2	0 Volts	20 BK

NOTES:

J117 SIGNAL CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J1-1	1	Bit #128	22 W-V
	A	J1-2	1	Bit #127	22 W-BL
	2	J1-3	1	Bit #126	22 W-G
	B	J1-4	1	Bit #125	22 W-Y
	3	J1-5	1	Bit #124	22 W-O
	C	J1-6	1	Bit #123	22 V
	4	J1-7	1	Bit #122	22 BL
	D	J1-8	1	Bit #121	22 W-O
	5	J1-9	1	Bit #120	22 Y
	E	J1-10	1	Bit #119	22 O
	6	J9-16	1	Hold Trigger Line	22 BR
	F	J4-1	1	68	22 W-BL
	7	J4-2	1	67	22 W-G
	G	J4-3	1	66	22 W-Y
	8	J4-4	1	65	22 W-O
	H	J4-5	1	64	22 V
	9	J4-6	1	63	22 BL
	I	J4-7	1	62	22 G
	10	J4-8	1	61	22 Y
	J	J4-9	1	60	22 W-V
	11	J4-10	1	59	22 W-BL
	K	J7-1	1	Bit #8	22 W-G
	12	J6-1	1	Bit #28	22 W-G
	L	J6-2	1	Bit #27	22 W-Y
	13	J6-3	1	Bit #26	22 W-O

NOTES: MS-3102A-36-404P

J117 SIGNAL CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	M	J6-4	1	Bit #25	22 V
	N	J6-5	1	Bit #24	22 BL
	O	J6-6	1	Bit #23	22 G
	P	J6-7	1	Bit #22	22 Y
	Q	J6-8	1	Bit #21	22 O
	R	J6-9	1	Bit #20	22 W-V
	S	J6-10	1	Bit #19	22 W-BL
	T	J6-11	1	Bit #18	22 W-G
	U	J6-12	1	Bit #17	22 W-Y
	V	J6-13	1	Bit #16	22 W-O
	W	J6-14	1	Bit #15	22 V
	X	J6-15	1	Bit #14	22 BL
	Y	J6-16	1	Bit #13	22 G
	Z	J6-17	1	Bit #12	22 Y
	1	J6-18	1	Bit #11	22 O
	2	J6-19	1	Bit #10	22 W-V
	3	J6-20	1	Bit #9	22 W-BL
	4	F3-2	2	-17 Volts	20 W-S
	5	J7-2	1	Bit #7	22 W-Y
	6	J7-3	1	Bit #6	22 W-O
	7	J7-4	1	Bit #5	22 V
	8	J7-5	1	Bit #4	22 BL
	9	J7-6	1	Bit #3	22 G
	10	J7-7	1	Bit #2	22 Y
	11	J7-8	1	Bit #1	22 O
NOTES: MS-3102A-36-404P					

J117 Signal Connector					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	+4.5	OVBUS-11		0 Volts	20 BK
	-4.5	OVBUS-12		0 Volts	20 BK
NOTES:					

J12 RECORDER CONTROL					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
1	J16-B		1	B-GE Input Line	Coax
2	J16-C		1	B-GE Input Line	Coax
3	J11-15		1	DLA Input	Coax
4	J11-17		1	DLA Input	Coax
5	J18-1		1	Recorder Output	Coax
6	J12-45		Jumper	0V	BK
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					
NOTES: Gnd all coax shields to the rack.					
				MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA	
				WIRE LIST	A 78W1A SHEET 57 OF SHEETS

J12 RECORDER CONTROL					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
26					
27					
28					
29					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
40					
41					
42					
43					
44					
45		0V-16	1		BK
46		J12-11	Jumper		BK
47		-20V-3	1		S
48					
49					
50					
NOTES: Chassis Gnd					
				MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA	
				WIRE LIST	A 78W1A SHEET 58 OF SHEETS

J18 RECORDER OUTPUT CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J12-9	1	Recorder Output	Coax
NOTES: Gnd Coax shield to Connector UG291/U with UG88/U MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA <b>WIRE LIST</b> A 178W11A SHEET 60 OF 60 SHEETS					

J17 RECORDER INPUT CONNECTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J11-49	1	Recorder Input	Coax
NOTES: Gnd. Coax Shield to Connector UG291/U with UG88/U MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA <b>WIRE LIST</b> A 178W11A SHEET 59 OF 60 SHEETS					

-20 VOLT BUS					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE
	1	J13-47	2	Power Supply -20V	20
	2	J13-48	2	Power Supply -20V	20
	3	J12-47	2	-20V Recorder Control	22
	4				
	5				
	6				
	7				
	8				
	9				
	10				
	11				
	12				
	13				
	14				
	15				
	16				
	17				
	18				
	19				
	20				
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A	46 OF SHEETS

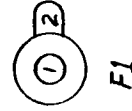
-85 VOLT BUS					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE
	1	J1-49	2	SR #1	22
	2	J2-49	2	SR #2	22
	3	J3-49	2	SR #3	22
	4	J4-49	2	SR #4	22
	5	J5-49	2	SR #5	22
	6	J6-49	2	SR #6	22
	7	J7-49	2	SR #7	22
	8	J13-49	2	Power Supply	20
	9	J9-49	2	Control	22
	10				
	11				
	12				
	13				
	14				
	15				
	16				
	17				
	18				
	19				
	20				
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A 78W11A	45 OF SHEETS

0 VOLT BUS					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J14-OV-10	2	OV	18 BK
	2	J14-OV-11	2	OV	18 BK
	3	J11-45	2	OV DLA	20 BK
	4	J11-46	2	OV DLA	20 BK
	5	J9-45	2	OV Control	20 BK
	6	J9-46	2	OV Control	20 BK
	7	J115 +4.5	2	OV V115	20 BK
	8	J115-4.5	2	OV J115	20 BK
	9	J116 +4.5	2	OV J116	20 BK
	10	J116 -4.5	2	OV J116	20 BK
	11	J117 +4.5	2	OV J117	20 BK
	12	J117 -4.5	2	OV J117	20 BK
	13	J13 -45	2	OV Power Supply	20 BK
	14	J13- 46	2	OV Power Supply	20 BK
	15	J16-A	2	Signal Connector	20 BK
	16	J12-45	1	OV Recorder Control	20 BK
	17				
	18				
	19				
	20				
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A	SHEET 48 OF SHEETS

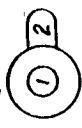
+12 VOLT BUS					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	J1-44	2	+12 Volt SR #1	20 R
	2	J2-44	2	+12 Volt SR #2	20 R
	3	J3-44	2	+12 Volt SR #3	20 R
	4	J4-44	2	+12 Volt SR #4	20 R
	5	J5-44	2	+12 Volt SR #5	20 R
	6	J6-44	2	+12 Volt SR #6	20 R
	7	J7-44	2	+12 Volt SR #7	20 R
	8				
	9	J9-44	2	+12 Volt Control	20 R
	10				
	11				
	12				
	13	J13-44		+12 Volt Supply	18 R
	14				
	15				
	16				
	17				
	18				
	19				
	20				
NOTES:					
MILGO ELECTRONIC CORPORATION MIAMI 47, FLORIDA					
WIRE LIST				A 78W11A	SHEET 47 OF SHEETS

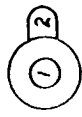
I1 POWER INDICATOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	K1-3	2	120VAC Switched	20 S
	2	TB2-3	2	120VAC (Common)	20 W
NOTES:					

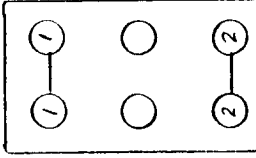
F1 FUSE					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
	1	SW1-2	2	120VAC (Hot)	12 S
	2	K1-1	2	120VAC (Fused)	12 S
NOTES:					





F3 -17V Fuse					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
1	J14-17-11	2	-17V (BS)	20	W/S
2	J117-22	2	-17V (OUT)	20	W/S
 F3					
NOTES:					

F2 FUSE					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
1	J15-B	2	120VAC (Common)	12	W
2	TB2-2	2	120VAC (Common)	12	W
 F2					
NOTES:					

SW1 BASE SWITCH					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
1	J15-A	2	120VAC (Hot)	12	S
2	F1-1	2	120VAC (Hot)	12	S
					
NOTES:					

BLOWER TBI					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE COLOR
1	K1-4	2	120VAC (Switched)	20	W/S
2	TB2-4	2	Blower	20	W
NOTES:					

TB2 (COMMON RETURN)					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
	1	F2-2	2	120VAC	12 W
	2	K1-B	2	120VAC (Contactor Coil Return)	20 W
	3	I1-2	2	Indicator	20 W
	3	J9-41	2	120VAC (Common)	22 W
	4	TB1-2	2	Blower	20 W
	5	J14-T903-2	2	SR (PS) Common	12 W
	6	J13-1	2	Control (PS) Common	18 W
	6	J11-36	2	DLA	18 W
NOTES:					

i K1 POWER CONTACTOR					
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE color
	1	F1-2	2	120VAC (Fused)	12 S
	2	J9-36	2	120VAC (Control)	20 S
	3	I1-1	2	Power Indicator	20 S
	4	J9-38	2	Control (Monitor)	22 W/S
	4	TB1-1	2	Blower (Hot)	20 W/S
	4	I1-1	2	Indicator Lamp	20 W/S
	5	J14-T903-1	2	Power Supply (-17V-20V)	12 W/S
	6	J13-4	2	Power Supply (-17V,-20V)	18 W/S
	6	J11-34	2	DLA (-85V)	18 W/S
	A	J9-29	2	120VAC (Contactor Coil)	20 W/S
	B			Contactor Coil	
K1					
NOTES:					

# **CHAPTER IX**

## **SCHEMATICS AND DIAGRAMS**

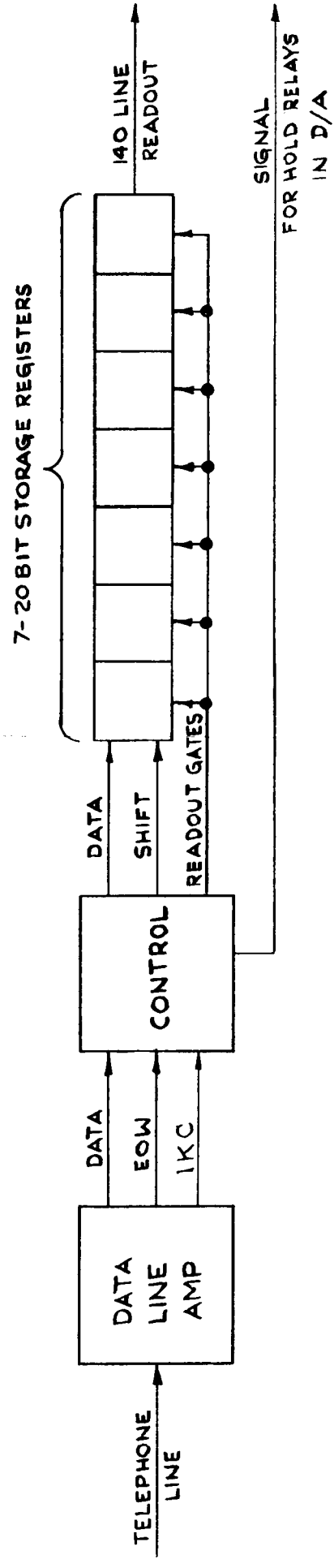


Figure 9-1 Block Diagram  
Model 78 Receiver Register

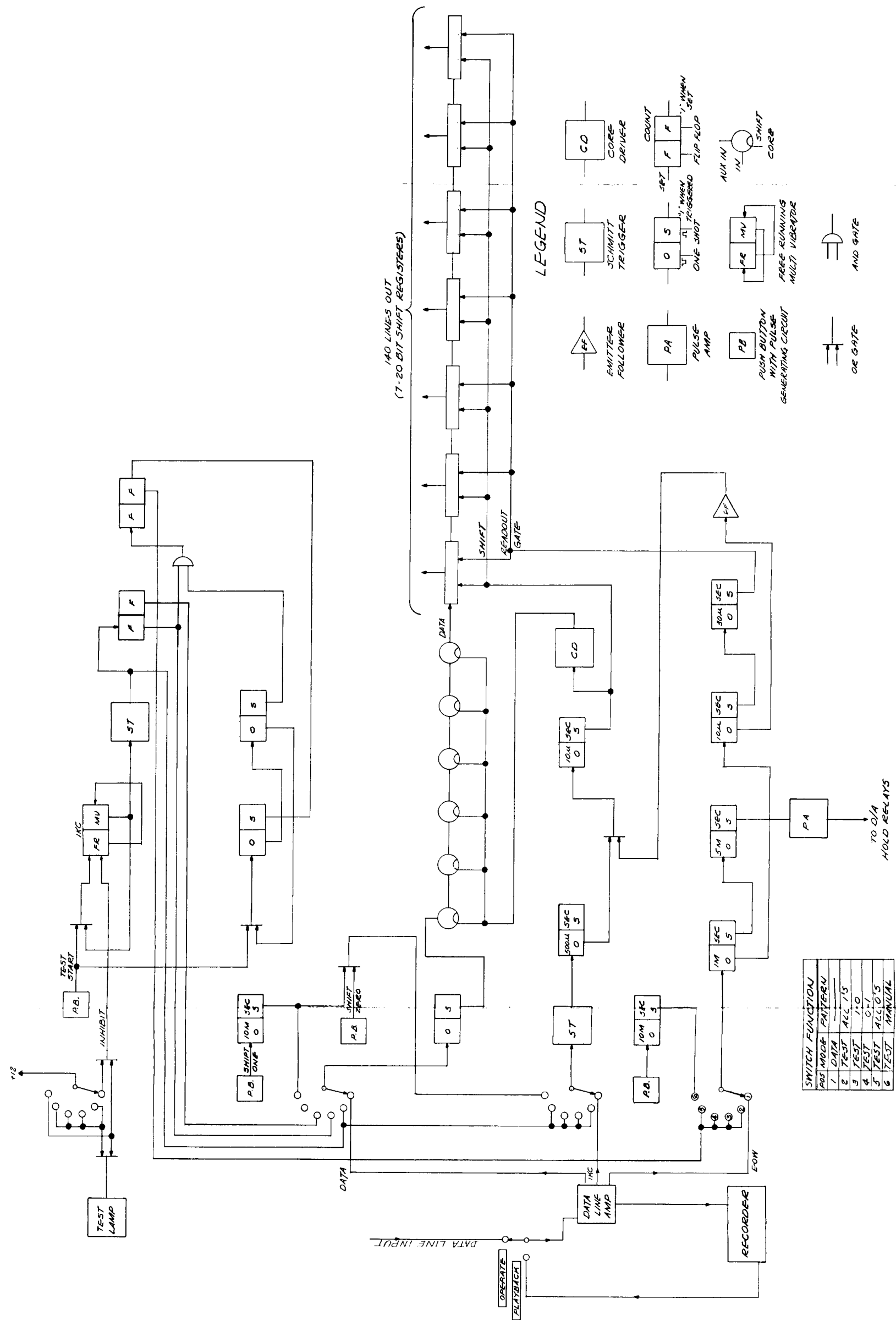


Figure 9-2 Logic Diagram  
MEC Model 78 Receiver Register  
Dwg. #D78B1A

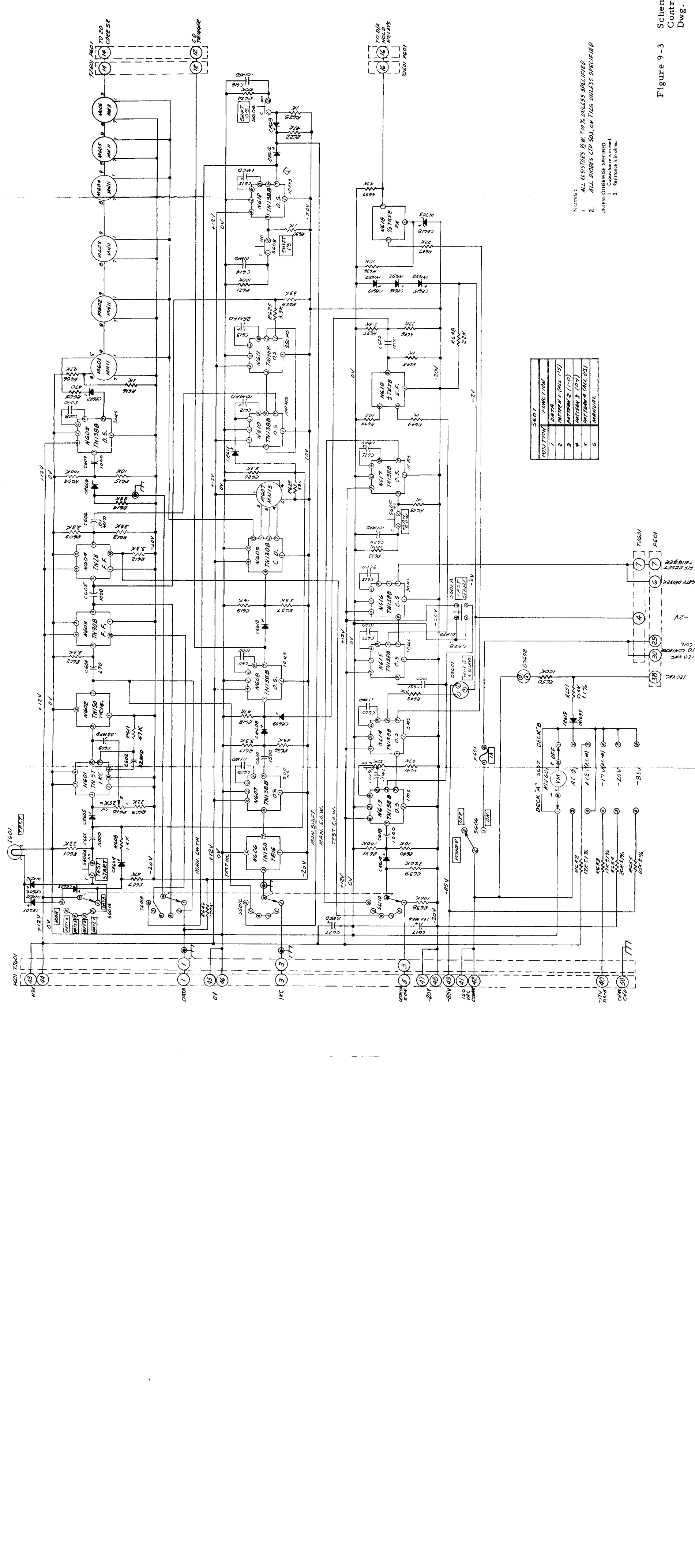
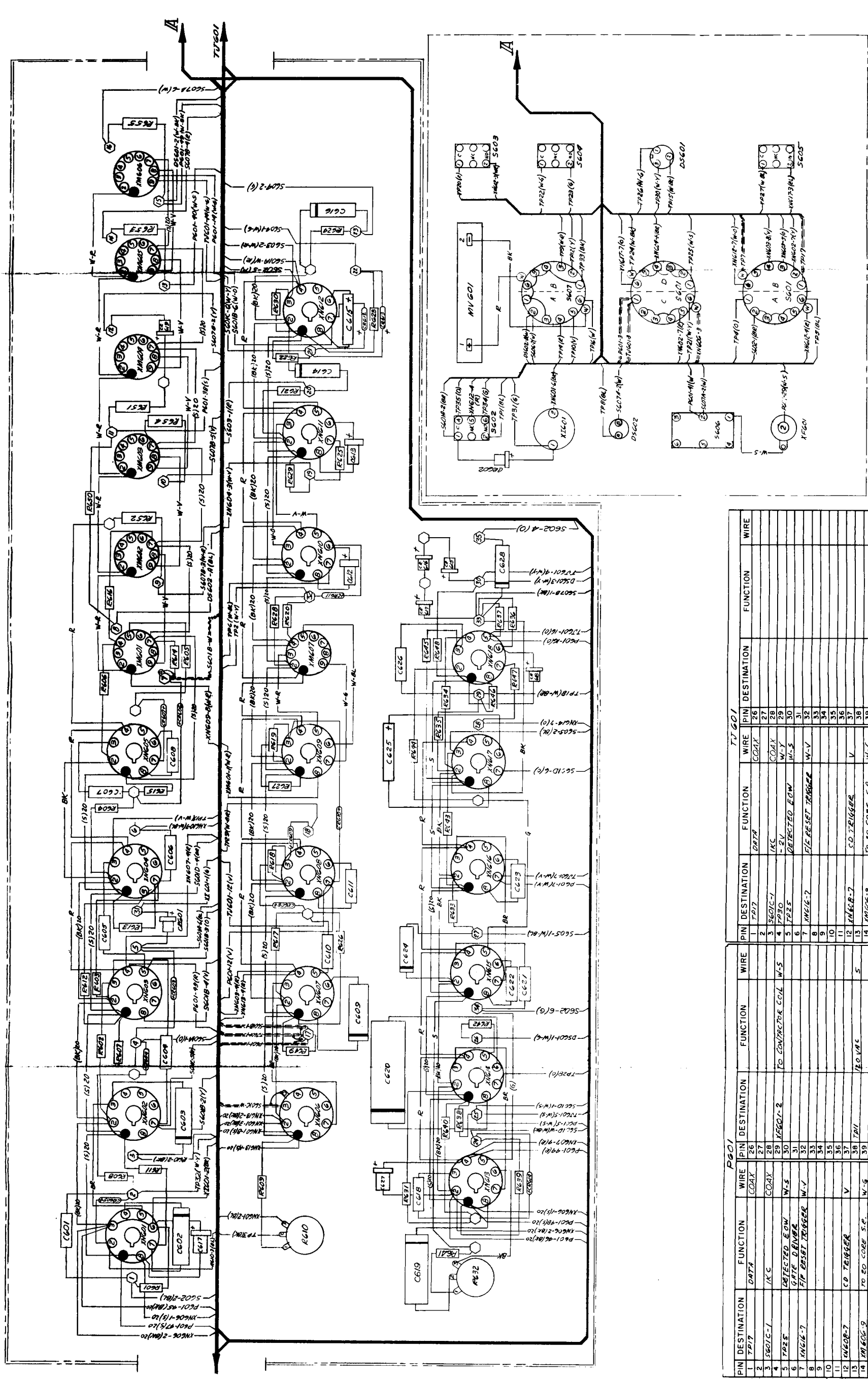


Figure 9-3  
Schematic  
Control Chassis  
Dwg. #D7856A  
9-7

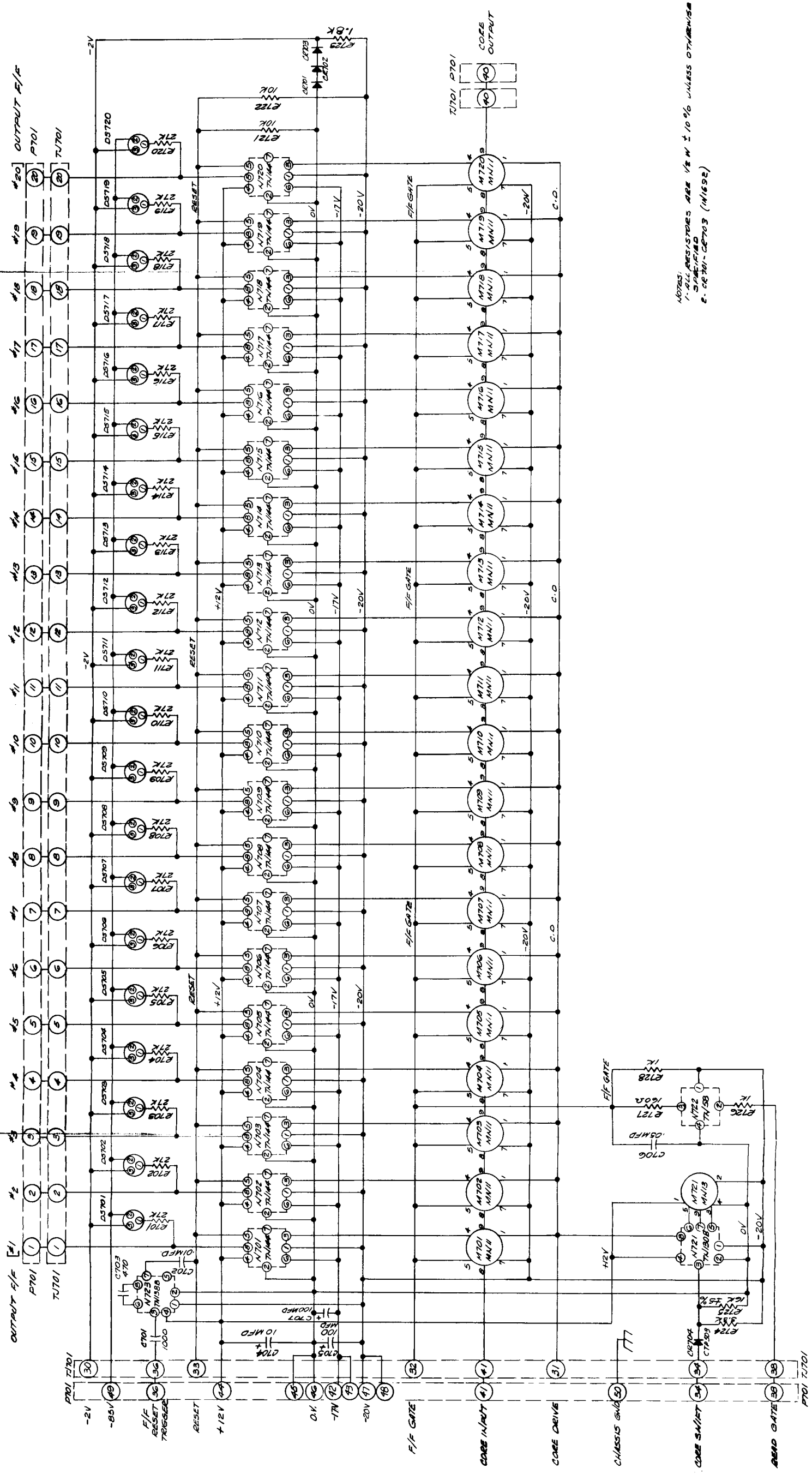


NOTES  
 1. ① INDICATES TEST POINT  
 2. WIRING PINS (41), (28), (30), (44), (46), (48), (50) ON P201  
 3. WIRING PINS (41), (28), (30), (44), (46), (48), (50) ON P201  
 4. WIRING PINS (41), (28), (30), (44), (46), (48), (50) ON P201

PIN DESTINATION	FUNCTION	WIRE	PIN DESTINATION	FUNCTION	WIRE	PIN DESTINATION	FUNCTION	WIRE
1	DATA	COAX	26	DATA	COAX	26	DATA	COAX
2	DATA	COAX	27	DATA	COAX	27	DATA	COAX
3	DATA	COAX	28	DATA	COAX	28	DATA	COAX
4	DATA	COAX	29	DATA	COAX	29	DATA	COAX
5	DATA	COAX	30	DATA	COAX	30	DATA	COAX
6	DATA	COAX	31	DATA	COAX	31	DATA	COAX
7	DATA	COAX	32	DATA	COAX	32	DATA	COAX
8	DATA	COAX	33	DATA	COAX	33	DATA	COAX
9	DATA	COAX	34	DATA	COAX	34	DATA	COAX
10	DATA	COAX	35	DATA	COAX	35	DATA	COAX
11	DATA	COAX	36	DATA	COAX	36	DATA	COAX
12	DATA	COAX	37	DATA	COAX	37	DATA	COAX
13	DATA	COAX	38	DATA	COAX	38	DATA	COAX
14	DATA	COAX	39	DATA	COAX	39	DATA	COAX
15	DATA	COAX	40	DATA	COAX	40	DATA	COAX
16	DATA	COAX	41	DATA	COAX	41	DATA	COAX
17	DATA	COAX	42	DATA	COAX	42	DATA	COAX
18	DATA	COAX	43	DATA	COAX	43	DATA	COAX
19	DATA	COAX	44	DATA	COAX	44	DATA	COAX
20	DATA	COAX	45	DATA	COAX	45	DATA	COAX
21	DATA	COAX	46	DATA	COAX	46	DATA	COAX
22	DATA	COAX	47	DATA	COAX	47	DATA	COAX
23	DATA	COAX	48	DATA	COAX	48	DATA	COAX
24	DATA	COAX	49	DATA	COAX	49	DATA	COAX
25	DATA	COAX	50	DATA	COAX	50	DATA	COAX

Figure 9-4  
 Wiring Diagram  
 Control Chassis  
 Dwg. #D78W6A





NOTES:  
 1. ALL RESISTORS ARE 1/2 W ± 10% UNLESS OTHERWISE SPECIFIED.  
 2. 2N7100-GE703 (M1692)

Figure 9-5 Schematic  
 20-Bit Shift Register  
 Dwg. #D76S7A

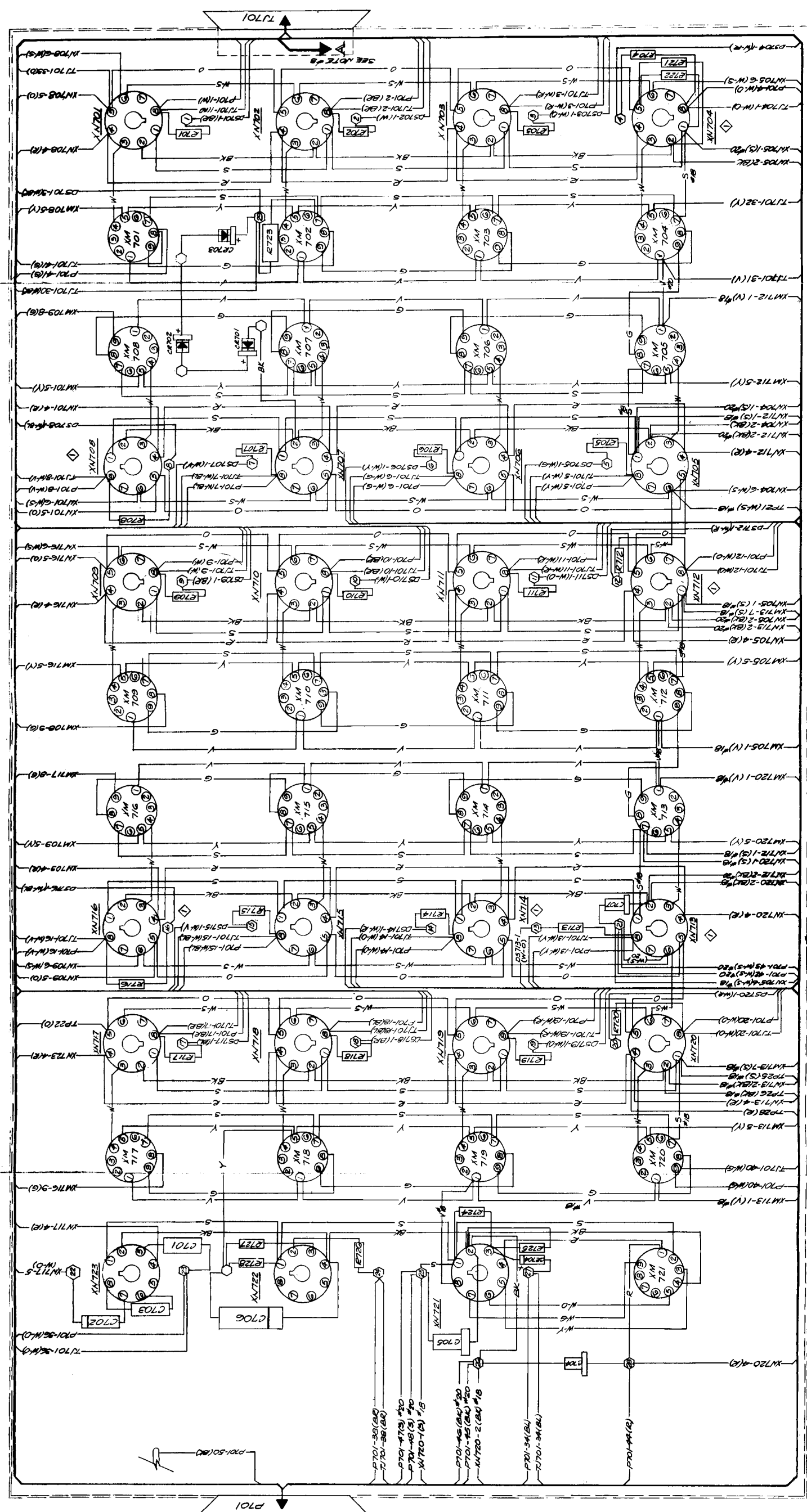
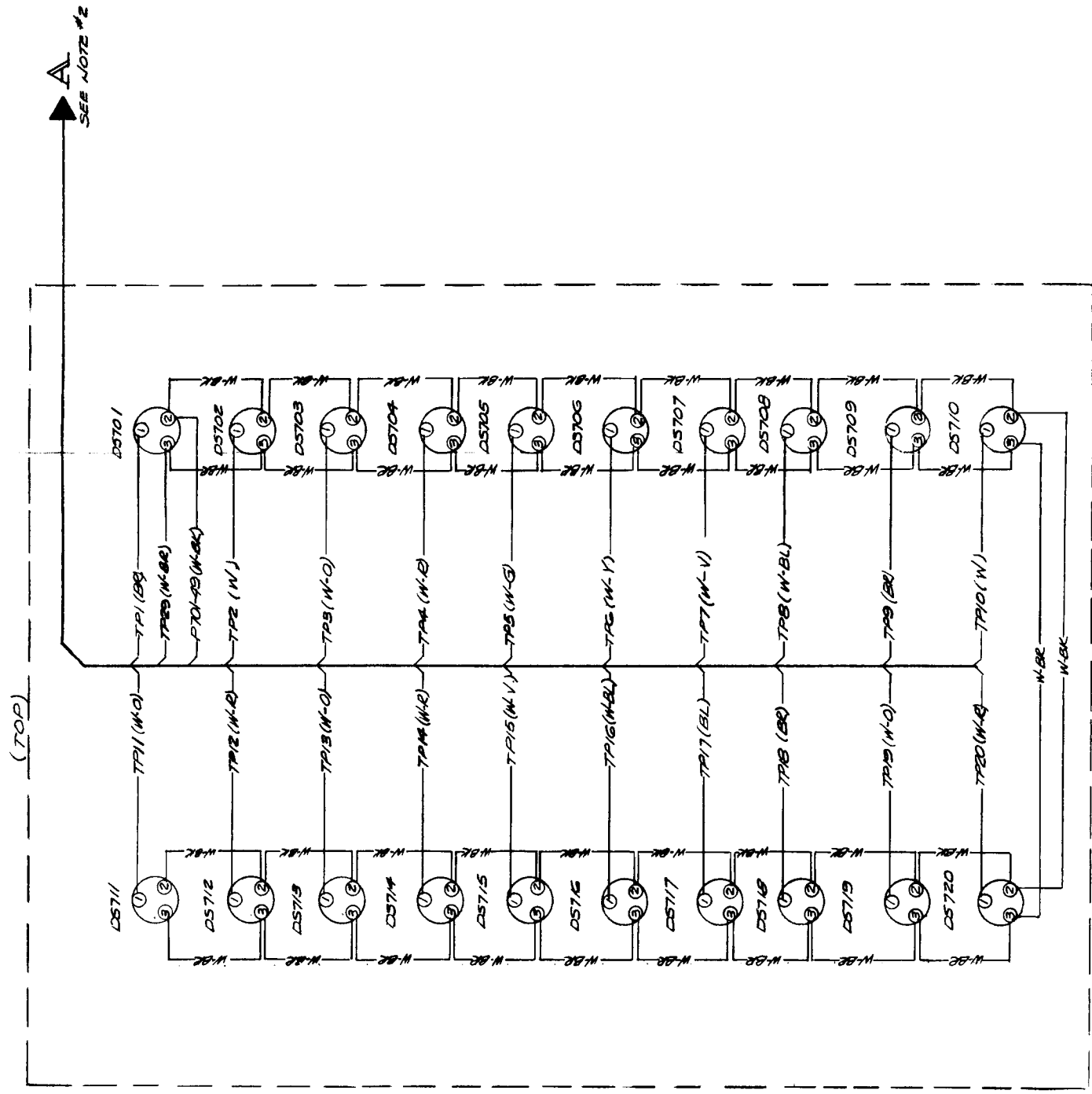


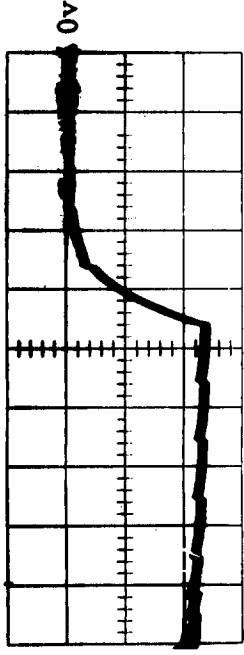
Figure 9-6  
Wiring Diagram  
20-Bit Shift Register  
Sh. 1 of 2 of Dwg. #76W7A

PLAN	DIST.	FUNCTION	WIRE	IN	DIST.	FUNCTION	WIRE	PLAN	DIST.	FUNCTION	WIRE
1	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	1	INT-10-B	INT-10-B	10
2	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	2	INT-10-B	INT-10-B	10
3	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	3	INT-10-B	INT-10-B	10
4	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	4	INT-10-B	INT-10-B	10
5	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	5	INT-10-B	INT-10-B	10
6	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	6	INT-10-B	INT-10-B	10
7	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	7	INT-10-B	INT-10-B	10
8	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	8	INT-10-B	INT-10-B	10
9	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	9	INT-10-B	INT-10-B	10
10	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	10	INT-10-B	INT-10-B	10
11	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	11	INT-10-B	INT-10-B	10
12	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	12	INT-10-B	INT-10-B	10
13	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	13	INT-10-B	INT-10-B	10
14	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	14	INT-10-B	INT-10-B	10
15	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	15	INT-10-B	INT-10-B	10
16	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	16	INT-10-B	INT-10-B	10
17	INT-10-B	INT-10-B	10	10	INT-10-B	10	10	17	INT-10-B	INT-10-B	10

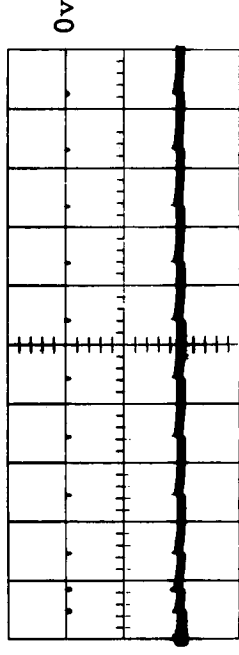
[illegible]



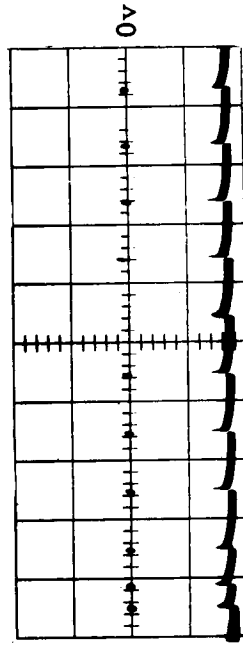
NOTES:  
 1. ALL WIRES ARE TO BE #22 GA UNLESS OTHERWISE SPECIFIED.  
 2. CABLE "A" CONTINUED ON SHEET 10F2



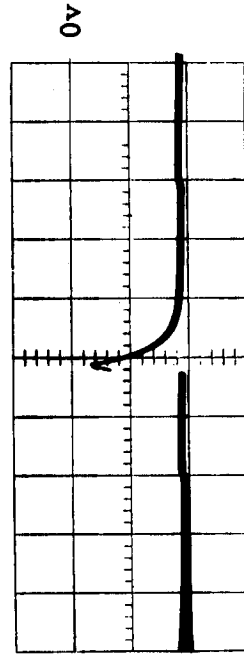
a. Signal to D-A Hold Relays  
5 volts per square  
1 millisecond per square



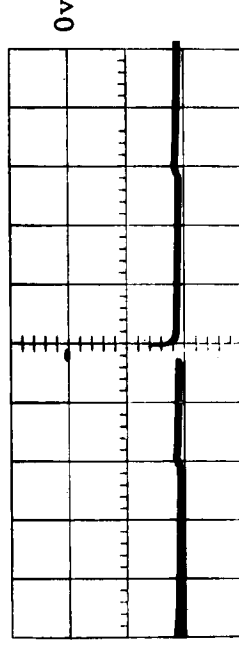
b. Core Drive Trigger to Shift Register Chassis  
10 volts per square  
1 millisecond per square



c. Data Pulses to Shift Register Chassis  
5 volts per square  
1 millisecond per square



d. Flip-Flop Gate  
10 volts per square  
200 microseconds per square



e. Output Data Levels  
10 volts per square  
200 microseconds per square

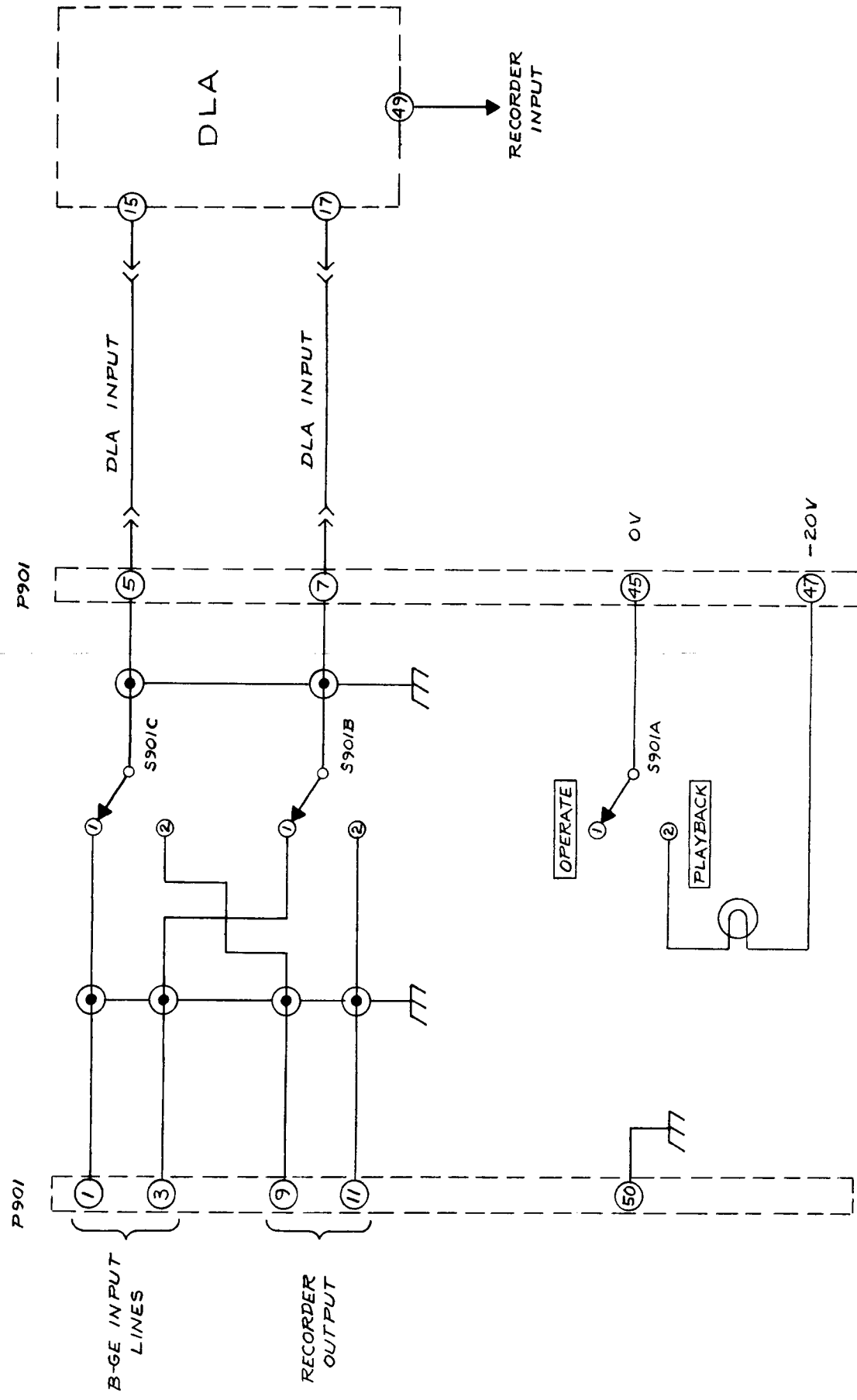


Figure 9-9. Schematic Recorder Control Dwg. #78S9A 9-19



## **CHAPTER X**

## **APPENDIX**

## **- 17 V AND - 20 V POWER SUPPLY**

### **MEC MODEL 76-9 A**

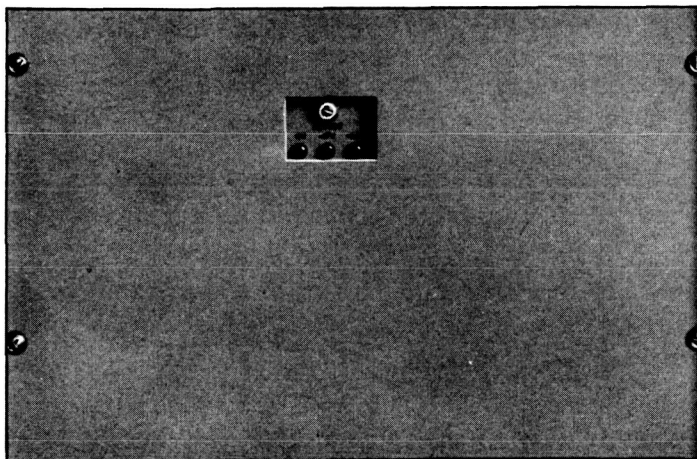
#### **1. GENERAL**

This power supply develops regulated output voltages of -17V at 40 amps and -20V at 3 amps. The -20V portion is developed by adding a -3V supply on the bottom of the -17V supply.

#### **2. -17V SUPPLY**

2-1. The 17V power supply is regulated by silicon controlled rectifiers (SCR) CR901 and CR902, by controlling the time which current can flow through their external circuit. When the external load is small, the SCRs are "on" for only a small amount of the input a-c cycle; when the external load is large, the SCRs are on for almost all of the input a-c cycle. The length of time which the SCRs are on is controlled by N901 (TN160) and its associated external circuitry.

2-2. CR901 and CR902 are SCRs which are phase-controlled elements used as a full wave rectifier element from the output of transformer T902. The two SCRs are fixed by gate signals from a common source, TN160. The operation of the circuit in TN160 is as follows: The unijunction transistor Q1 acts as a relaxation oscillator synchronized by its inter-base voltage supply. The firing circuit (TN160) is connected to the output of a single phase bridge formed by diodes CR904, CR905, CR906 and CR907, through R906. Zener diode (CR1) in the TN160 clips the rectified voltage, which charges capacitor C907 through resistor R7 in TN160. This voltage fires the unijunction transistor and whichever SCR has a positive anode voltage during that half cycle of the a-c input. Upon firing, the voltage across the SCRs decrease to the forward conduction value of less than 1 volt. This discharges capacitor C907, and keeps it discharged until the a-c input is reversed, at which time a new timing cycle starts for



-17v and -20v Power Supply

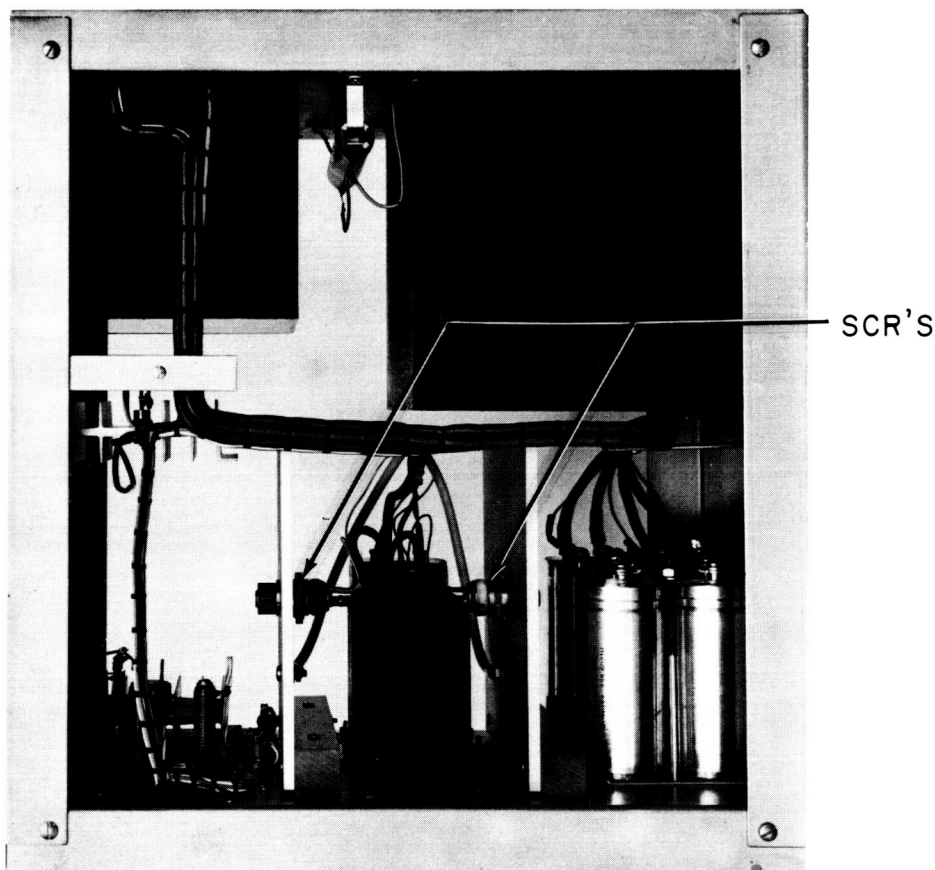


the alternate SCR. If no current is being shunted by the voltage control circuit (Q2 and its associated circuitry) through R6, Q1 will fire within ten degrees after the beginning of each half cycle of the a-c supply voltage. At this minimum firing angle, the SCRs will deliver the maximum voltage to the load.

2-3. Q2 controls the firing angle by shunting C907. An increase of base current of Q2 will decrease the effective resistance of Q2, which will add a loading to C907, changing the charging time constant. This diversion of current will retard the firing angle so that a very small output will occur from CR901 and CR902.

2-4. DETAILED DESCRIPTION - The base current of Q2 is a feedback signal (or error voltage) developed from comparing a voltage on the base of Q2 (which is proportional to the output voltage) and a reference voltage across zener diode CR2 in the TN160. If the voltage tries to rise, more base current flows in Q2, resulting in more collector current. More collector current in Q2 will result in C907 taking longer to charge, and will therefore delay the time of the peak voltage on Q1. (the peak voltage on Q1 is the voltage necessary to fire Q1). This retards the firing angle and returns the output voltage to normal. If the output voltage drops, the reverse action takes place.

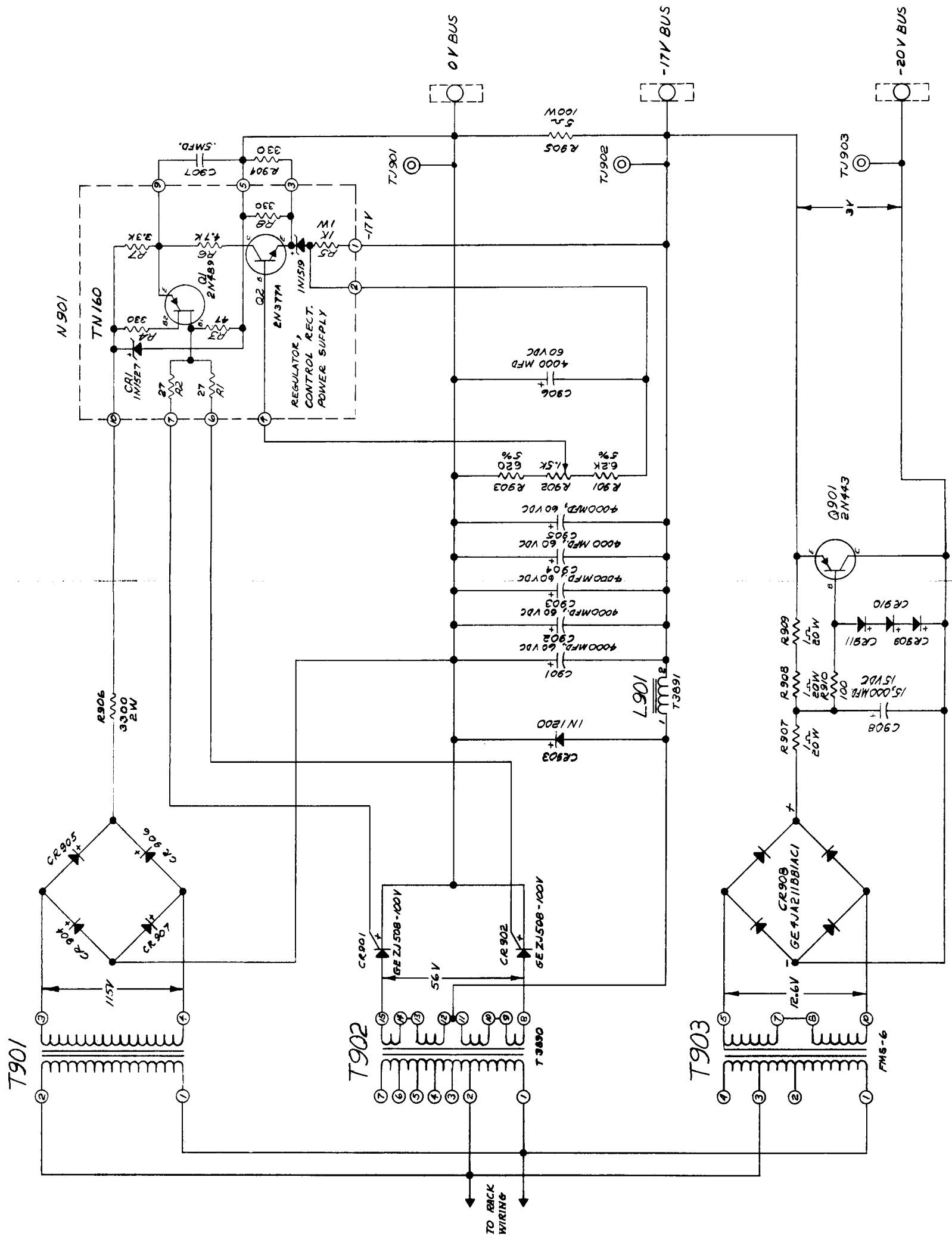
2-5. C906 and R5 are to increase stability in the feedback circuit. CR903 acts as a free wheeling diode to maintain current in the load and filter choke when the SCRs are both blocking. It contributes to over-all circuit stability. R905 is a minimum load. L901 and C901 through C905 are the filter section.



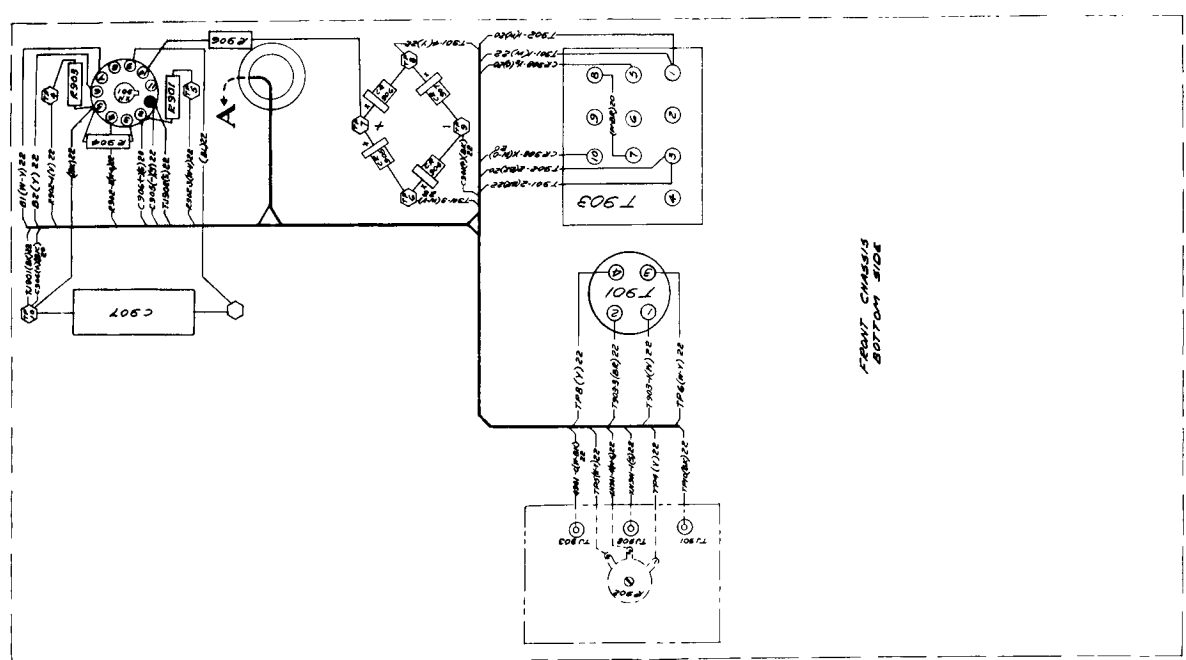
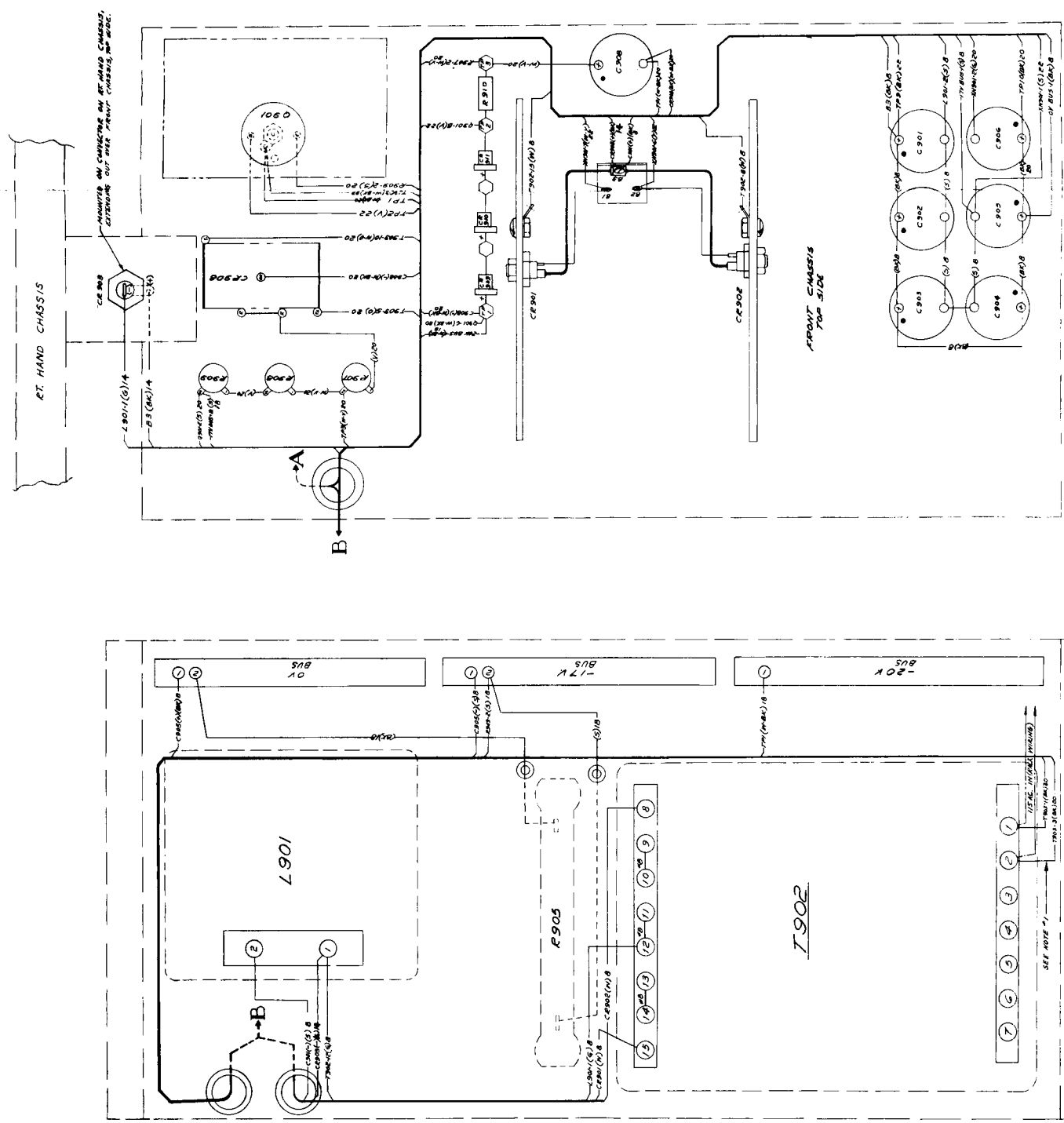
Power Supply, Bottom View, Showing Silicon-Controlled Rectifiers

### 3. -20V SUPPLY

The -20V supply is only a -3V supply added on the bottom of the -17V supply. The voltage is rectified by CR908 and filtered by R907 and C908. Since the forward drop through silicon diodes are approximately constant through a large change of current, CR909, CR910 and CR911 are used as a voltage reference. Q901 acts as a shunt regulator, since its emitter voltage will be only about 0.3 volts from its base voltage, which is constant. Therefore the output voltage across Q901 is constant within the current rating of the supply. A constant current is flowing through R907, R908 and R909. When there is no external load, this current flows through Q901, but when there is an external load, current which flows through the external load is subtracted from the current flowing through Q901. R910 provides current for CR909, CR910 and CR911.



NOTES:  
 1. ALL RESISTORS  $\pm 10\%$ ,  $\frac{1}{2}W$  UNLESS OTHERWISE SPECIFIED.  
 2. ALL DIODES #1N1692 UNLESS OTHERWISE SPECIFIED.



NOTE:  
1. LEAVE WIRES ON TERMINAL 2 LONG  
ENOUGH TO REACH TERMINAL #7

Wiring Diagram  
-20v, -17v Power Supply  
Dwg. #76W3A

# TRANSISTOR POWER SUPPLY

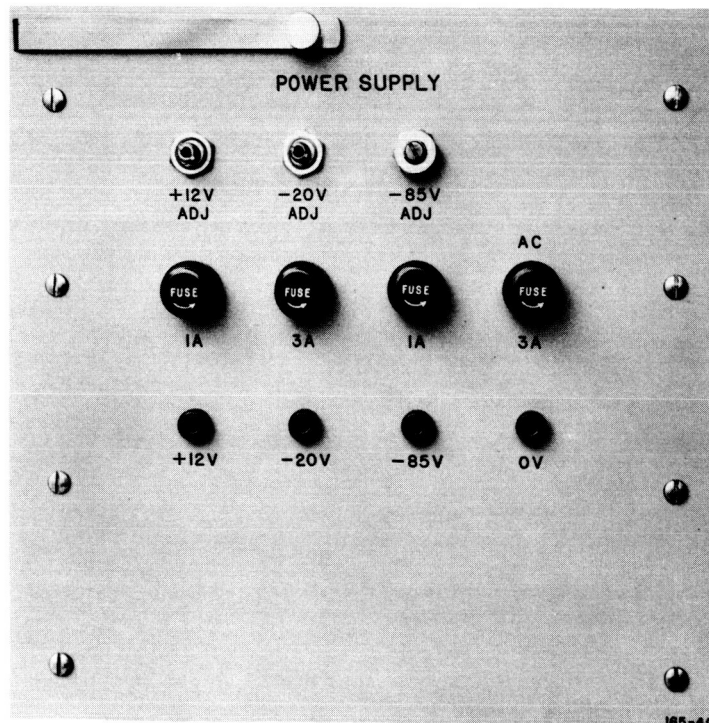
## MEC MODEL 165-4 C

### 1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v ( $\pm 5v$ ) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

### 2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.



Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414, and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

### 3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant

output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts

more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

#### 4. -65v SUPPLY

4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

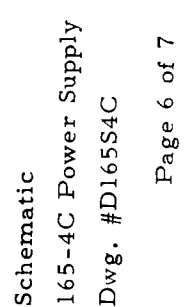
4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive

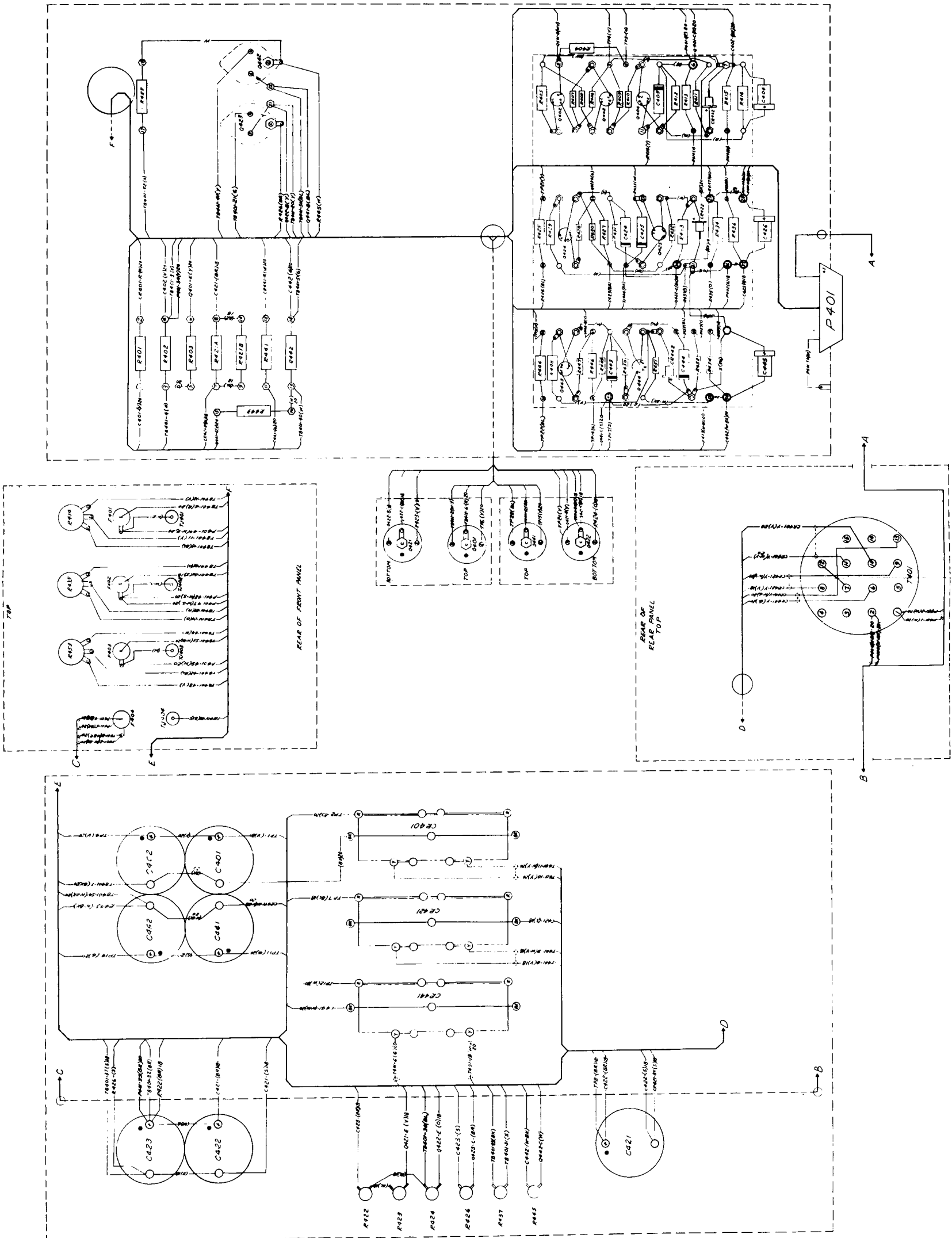


with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.



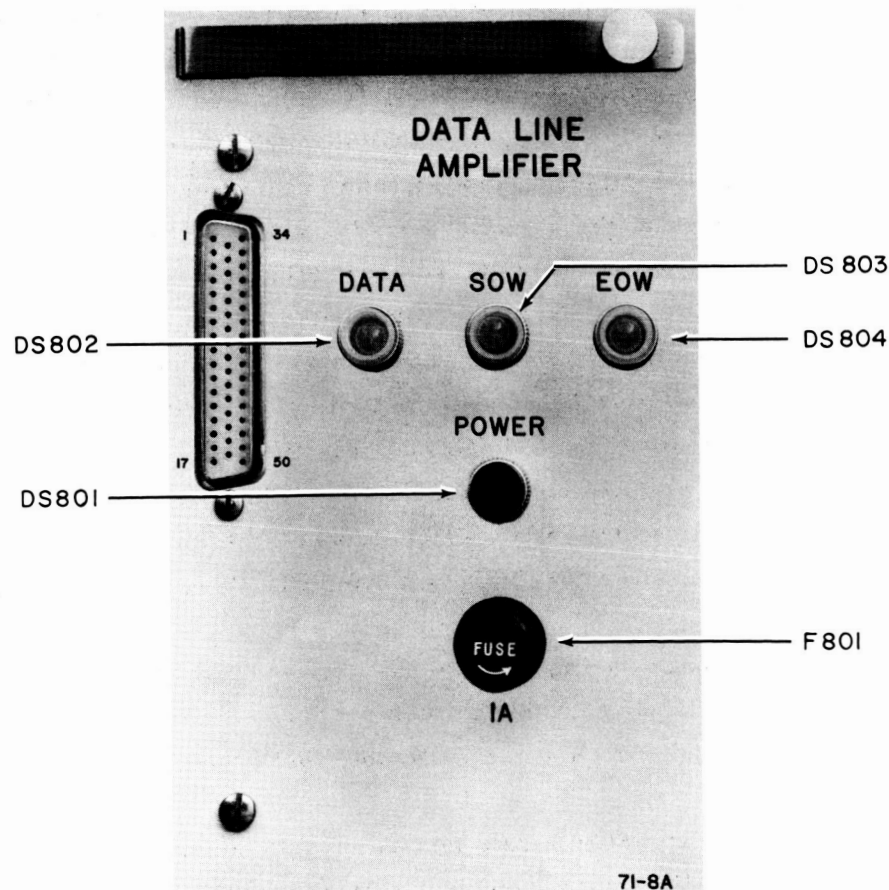
NOTES  
1. ALL WIRING UNLESS SPECIFIED  
2. ALL WIRING TO BE PRINTED IN WIRE



# DATA LINE AMPLIFIER MEC MODEL 71-8 A

## 1. GENERAL

1-1. The Data Line Amplifier receives data in the form of modulated tone bursts of approximately 2 kc at a 1 kc repetition rate from 3 kc voice channels on balanced or unbalanced communication lines, equalized for 1 kc data bit rate. The tone bursts for data are 0.5 milliseconds. The bursts for Start of Word (SOW) and End of Word (EOW) may vary in length depending on the system in which the Data Line Amplifier is used. In some systems, SOW and/or EOW may not be used. The outputs are a 1 kc sinusoidal waveform which is synchronized to data, and pulse outputs of 10 to 20 volts, depending upon termination, approximately 10 microseconds wide, for data, SOW, and EOW. The pulse outputs are cathode follower outputs and require terminating resistors external to the chassis. The Data Line Amplifier Input-Output Relationships figure shows the relationships of incoming and outgoing data. The unit operates on 115 volts  $\pm$  10 vac and has a self contained power supply for generating regulated +250 volts and -250 volts for use within the chassis.



Data Line Amplifier

## 2. DETAILED DESCRIPTION

2-1. Incoming Signals - Data enters the chassis in the form described in paragraph 1-1, at pins 15 and 17 of P801. The inputs are connected to pins 1 and 2 of the bridging transformer T801, which has a 10,000 ohm input impedance. External resistors must be used to match the communication line impedance, normally 600 ohms. This makes it possible for one or more receiving line amplifiers to be used on a single circuit, if so desired. The signal is then filtered in a band pass filter for noise rejection before entering the first stage of amplification. The incoming signal can be seen unfiltered at TJ801, pin 16. However, at this point, the circuit is loaded with the filter impedance and does not give a true representation. The filtered signal can be seen at TJ801, pin 50. Potentiometer R801 provides level selection of the incoming signal to the amplifier and is nominally set for a signal swing of approximately 0.5 volts peak to peak at pin 2 of R801. The filtered signal is a-c coupled to the control grid, pin 1, of V801. This is a remote cut-off pentode tube with AGC applied as bias to the control grid through R802. The signal at the output, pin 5 of V801, is a-c coupled to the grid (pin 2) of V802A which provides the second stage of amplification. The output of V802A pin 1, drives a phase splitter, V802B at pin 7, which has outputs at pins 8 and 6 which are out of phase; that is, when pin 6 is going positive, pin 8 is going negative and vice versa. An output at the junction of R812 and R882 in the cathode of V802B is provided for purposes of recording the data on tape. Each output of the phase splitter drives one-half of V803, a push-pull amplifying stage with a common cathode resistor, R816. The outputs of V803, pins 1 and 6, drive the detector, composed of diodes CR801, CR802, and related circuitry. The anodes of these diodes are clamped to 0 volts by diode CR803. Potentiometer R822 determines the d-c bias at the cathodes of the detecting diodes, and in this way determines the amount of the negative going a-c component of the signal from V803 which will appear at the grid, pin 2 of V804A. V804A is an amplifier which is biased near full conduction by R883 and CR803 which clamps the grid voltage to 0 volts. Negative going pulses from pin 1 or 6 of V803, which exceed the bias voltage determined by R822, cause diode CR801 or CR802 to conduct, turning off V804A and producing a positive pulse at its output, pin 1. Negative pulses at the diode detector output also conduct through diode CR804, are filtered, and applied to the grid of V801, the first stage of the amplifier, for AGC action. The detected signal at the output of V804A is amplified and inverted by V804B which drives the logic circuitry. The waveforms of the detected signal are shown in the Data Line Amplifier Waveform Figure.

2-2. Logic - The negative going edge of the detected signal triggers the data one-shot, V805, a 450 microsecond one-shot, which in turn produces a positive going pulse at pin 6 triggering the SOW one-shot V806, and the EOW one-shot V807; three conditions are now possible:

a. The incoming signal is a data burst. In this case, the data one-shot V805, completes its time delay in 450 microseconds and triggers off the SOW and EOW one-shots as pin 6 of V805 goes negative.

b. The incoming signal is a SOW burst. In this case, the data one-shot continues to receive negative pulses and does not complete its time delay in 450 microseconds. The SOW one-shot V806, is not triggered off, but completes its time delay at a time determined by R849 (normally 2 milliseconds). The EOW one-shot V807, is triggered off by the data one-shot because the incoming code burst has ended (normally 2.5 milliseconds) before the EOW one-shot could complete its time delay.

c. The incoming signal is an EOW burst. When the data one-shot is held on for that duration, both the SOW and EOW one-shots complete their time delays before the data one-shot can trigger them off. The period of the EOW one-shot is determined by R843 and is normally 4 milliseconds.

2-3. As the SOW one-shot is triggered on for every data code burst, its output at pin 6 is used to drive the data output cathode follower at pin 7 of V808. This reduces loading on the data one-shot. The grid of the data cathode follower is biased at approximately -25 volts. The cathode is normally returned through an external resistor to -20 volts. The cathode follower will now conduct when positive pulses occur at the grid, producing a positive output pulse approximately 10 microseconds wide at the mid-point and 20 volts in amplitude, each time there is an incoming data burst, SOW burst, or EOW burst. A neon indicator, DS802, connected to the plate, pin 1, of the data one-shot V805, indicates when data is triggering the data one-shot. This data indicator glows faintly during data absence, but increases in intensity when data is present.

2-4. SOW is recognized by the fact that the SOW one-shot has completed its time delay before the data one-shot has returned to its quiescent state (this will occur for both incoming SOW and EOW). When the incoming signal consists of data bursts, and the SOW one-shot is being triggered on by the leading edge of the data one-shot, and off by the trailing edge, the two one-shot waveforms have basically the same width. The negative going pulse from the data one-shot, pin 1 of V805, is connected to the plate of CR806, which is one leg of a diode gate for detecting SOW. The positive going pulse from the SOW one-shot, pin 6 of V806, is connected to the plate of CR805, which is the remaining leg of the gate for recognizing SOW. When the two pulses to CR805 and CR806 have the same width, the junction of the two diodes is maintained positive, keeping the grid of V810B, pin 7, at a voltage which will retain that half of the tube in full conduction, as diode CR811 clamps the voltage to the grid at 0 volts. Capacitors C817 and C825 filter spikes that occur as a result of slight discrepancies of switching times. When an SOW burst occurs, the SOW one-shot completes its time delay, but the data one-shot is still on. This situation produces a voltage which is approximately +20 volts at the plates of both CR805 and CR806, causing the junction of the two diodes to drop to approximately 20 volts where normally one of the two one-shots had maintained this point at approximately +200 volts. The voltage divider consisting of R834, R835, and R863, which is returned to -250 volts, now produces a negative voltage at the grid (pin 7) of V810

turning the tube off and producing a positive pulse at pin 6, the output. After differentiation, this pulse drives a cathode follower, V808A, which is identical to the data cathode follower just discussed. A neon indicator at the plate, pin 6, of V810B indicates when SOW has been detected. The SOW gate will recognize the same set of circumstances for EOW, as this produces the same condition of the SOW one-shot time delay, ending before the incoming code burst allows the data one-shot to return to its quiescent state.

2-5. EOW is recognized in a similar manner as SOW. The EOW one-shot V807, is triggered on and off by the data one-shot which applies positive and negative pulses at its grid, pin 2. As this one-shot is set for a period exceeding that of the SOW one-shot, when a SOW burst occurs, it will not have completed its time delay before the data one-shot recovers from the SOW burst. On an EOW burst, the same circumstances are produced with the EOW one-shot as just described for the SOW one-shot. The data one-shot produces a negative pulse to the plate of diode CR807, as it did to CR806. The EOW one-shot produces a positive pulse to the plate of diode CR808. During data bursts, the EOW one-shot is triggered off by the data one-shot, and both pulses are of approximately the same width. When an EOW burst occurs, the data one-shot is kept on, and the EOW one-shot completes its time delay. This produces a negative pulse to the grid (pin 2) of V809A similar to that previously discussed for SOW. The output at pin 1 of V809 is a positive pulse for EOW recognition, which drives pin 7 of V809B, the EOW output cathode follower. This cathode follower is identical to the data and SOW cathode followers. A neon indicator is connected to the plate of V809A which indicates the detection of EOW.

2-6. Oscillator - The oscillator within the Data Line Amplifier provides a 1 kc sine wave synchronized to data, and is used by external sources as a means of determining the data bit rate, often referred to as clock. This is necessary as an accurate means of determining whether an absence of data represents one or more 0 bits.

2-6.1. The basic oscillator, V810A, is similar to a standard Colpitts configuration. The frequency is varied by adjusting variable inductor L803. The oscillator is synchronized to incoming data by V811B. Each time a data bit is recognized, one-shot V806 is triggered. Its output, a positive pulse at pin 6, pulses V811B through capacitor C816. Since inductor L803 is in series with the cathode of V811B, each time the tube is pulsed, current flowing through the tube also flows through L803, which is within the tuned circuit of the oscillator. The output of the oscillator, at pin 3, drives a cathode follower, V811A, whose output at pin 3 is a-c coupled to the output terminal, pin 7 of P801, as 1 kc output.

2-7. Power Supply - 115 vac enters the Data Line Amplifier at pins 34 through 37 of P801. DS801 indicates when power is on. The a-c power is connected through fuse F1 to the primary of transformer T802. A secondary, pins 3 and 5, provides 6.3 vac for tube filaments.

are best determined by examining the detected waveform output, TJ801-48. It is convenient for the remainder of the adjustments to use the delayed sweep feature of the oscilloscope. Using EOW, TJ801-9, as sync, and the delayed sweep, it is possible to examine incoming data occurring over a relatively long period at magnifications where the full sweep displays only a few milliseconds of data, and the scope still maintains sync on a stable source. The level and detection controls, potentiometers R801 and R822, should be adjusted until the detected waveform TJ801-48, has the appearance shown in the Data Line Amplifier Waveform Figure. The detected waveform is nominally a 15 to 20 volt negative pulse. It can be noted that for each bit of data, the ideal waveform produces two negative pulses, each with full amplitude, and squared at the bottom. It is also acceptable and common, due to frequency rolling, to have one of the two pulses of a lesser amplitude. It is unacceptable to have three pulses, specifically because the data one-shot is re-triggered on the third pulse making the output of V805 excessively wide. Proper adjustment, therefore, constitutes the obtaining of maximum amplitude and squareness of the detected signal without detecting three pulses for a data bit. If the adjustments have been made properly, one data pulse will appear at TJ801-13 for each data burst on the input at TJ801-50.

2-8.3. SOW and EOW One-Shots - The SOW and EOW one-shots are variable because the length of the SOW and EOW code bursts depend upon the system in which the Data Line Amplifier is used. These one-shots are normally set for a period that produces a pulse which is 0.5 milliseconds shorter than the incoming code burst for that signal. For example, if SOW is a 2.5 millisecond burst, the SOW one-shot is adjusted for 2 milliseconds. If EOW is a 4.5 millisecond burst, the EOW one-shot is adjusted for 4 milliseconds.

2-8.3.1. To properly adjust the SOW one-shot, using the delayed sweep of the oscilloscope as previously described, synchronize on EOW at TJ801-9 in the Data Line Amplifier. On one trace observe the data input, TJ801-50. On the remaining trace observe the SOW one-shot, TJ801-44. Adjust the time delay of the scope sweep until a SOW burst is seen. It is necessary to observe the one-shot pulse occurring during the SOW burst because during a data burst the SOW one-shot is triggered off by the data one-shot and not allowed to complete its time delay. Adjust potentiometer R849 to set the SOW one-shot for the desired width. Adjust the time delay of the scope until an EOW burst is seen. Observe the EOW one-shot, TJ801-46 and set potentiometer R843 for the desired width.



A secondary, pins 8 and 10, provides 600 vac center tapped at pin 9 to 0 volts. Three diodes in series are used for rectification to safely meet the voltage requirements. Diodes CR816 through CR821 provide full wave rectification for +250 volts. Resistors R873, R878, and R879 and capacitors C834A and C834B provide filtering. Regulation of the +250 volts is performed by two VR tubes in series, V814 and V815. Half wave rectification, via diodes CR822 through CR824, is used for -250 volts. Filtering and regulation are similar to the +250 volt supply.

2-8. Adjustment - Three basic types of adjustments are to be made on the Data Line Amplifier.

2-8.1. Oscillator - The oscillator frequency is adjusted to 1 kc by adjusting variable inductor L803. Before the oscillator can be properly adjusted, the synchronizing effect of incoming data must be removed. One method of accomplishing this is to adjust R801 until the center tap is at 0 volts. The oscillator no longer receives sync pulses and is then in a free-running condition. Using a dual-trace oscilloscope such as a Tektronix 545A with CA plug-in, synchronize and put one trace on a good 1 kc source. If a local source is not available, data from a Data Line Amplifier, preferably with an input test pattern of all "1"s offers a suitable source. Use the remaining trace to observe pin 3 of tube V810. L803 should be adjusted to produce a frequency equal to the test frequency. By ultimately using a sweep on the scope which displays only one or two cycles, the operator can insure that the two signals are actually at the same frequency.

#### NOTE

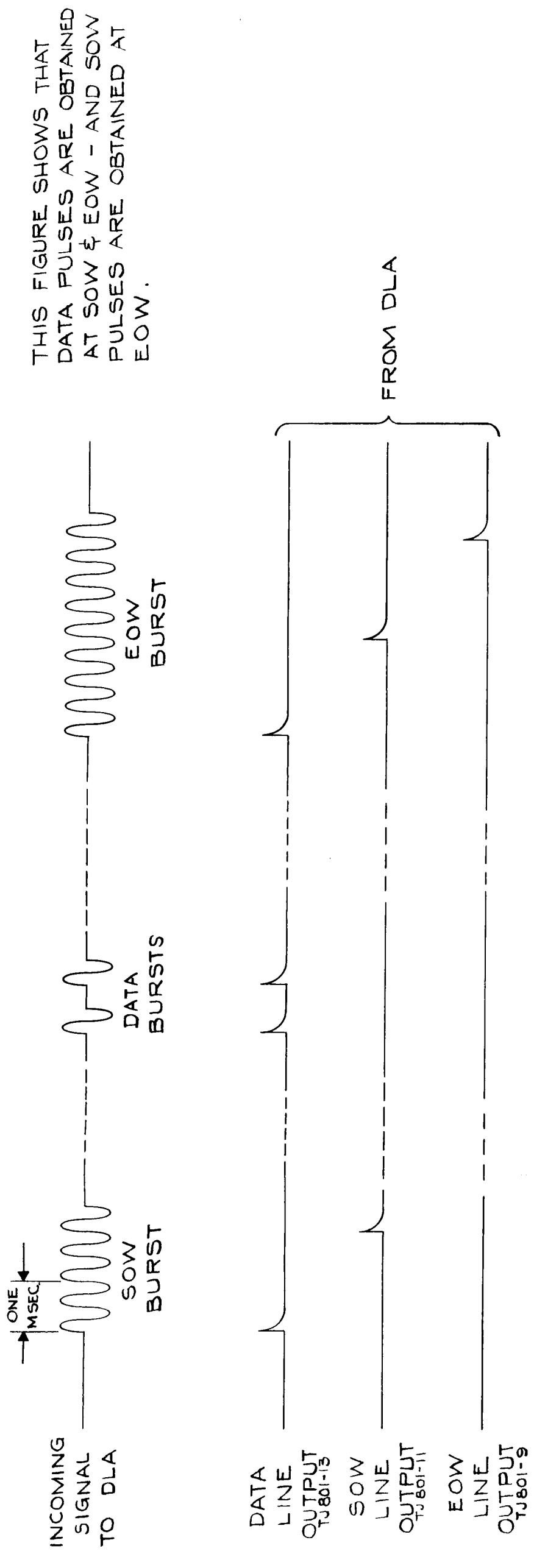
At relatively slow sweeps, the two waveforms may have the appearance of being synchronized. If going to a faster sweep results in double traces, the two waveforms are not yet synchronized.

Rolling of one trace with respect to the other should be expected, but it is readily possible to adjust the oscillator to within a few cycles per second of the external source. A normal adjustment of  $\pm 3$  cps is satisfactory.

#### NOTE

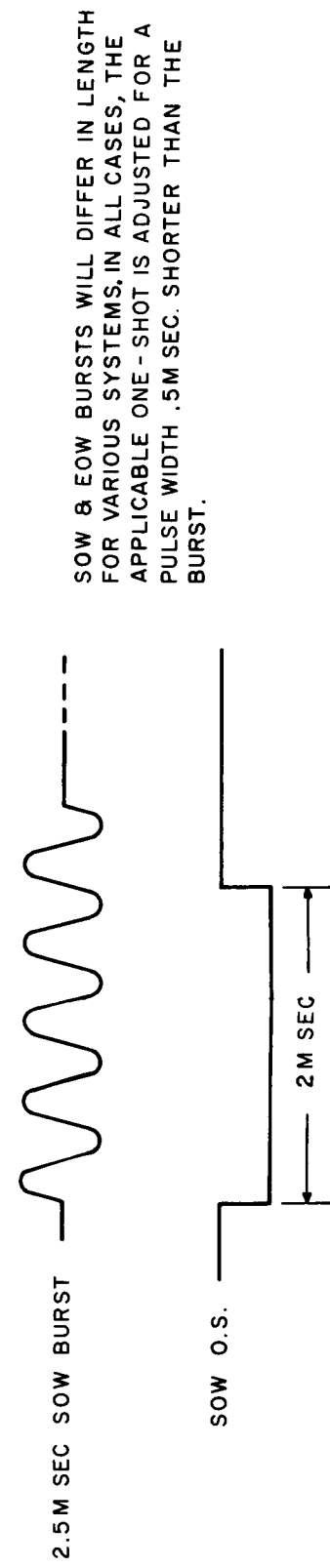
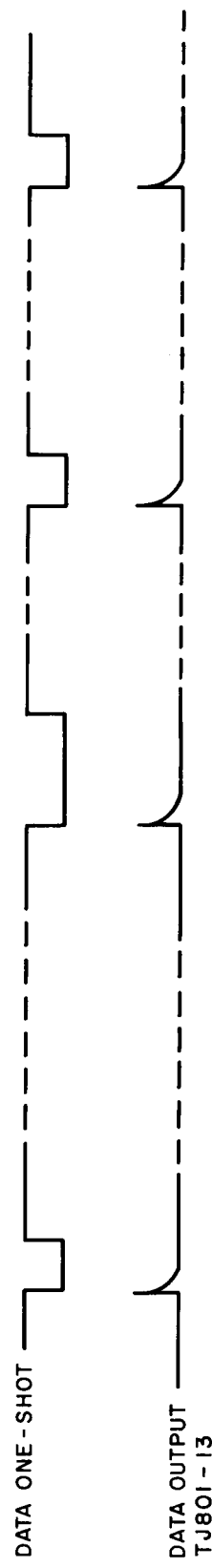
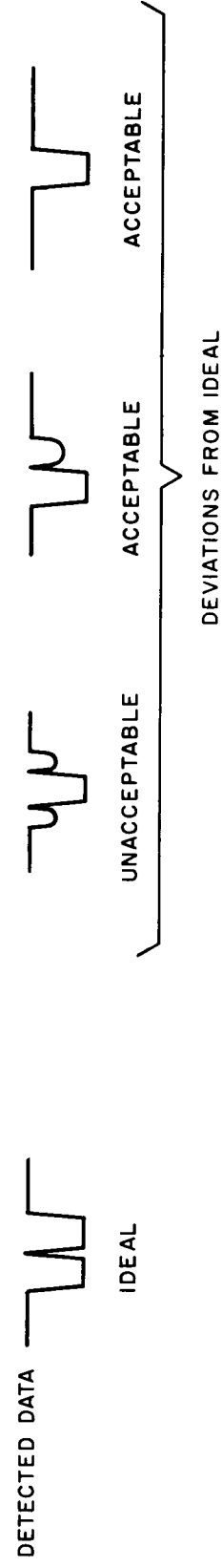
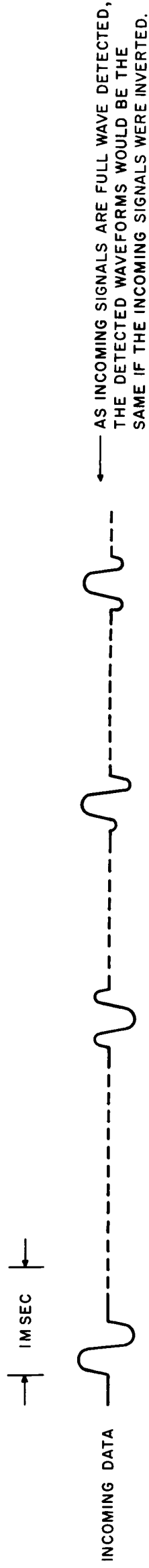
An alternate method of adjusting the oscillator using a frequency counter is acceptable.

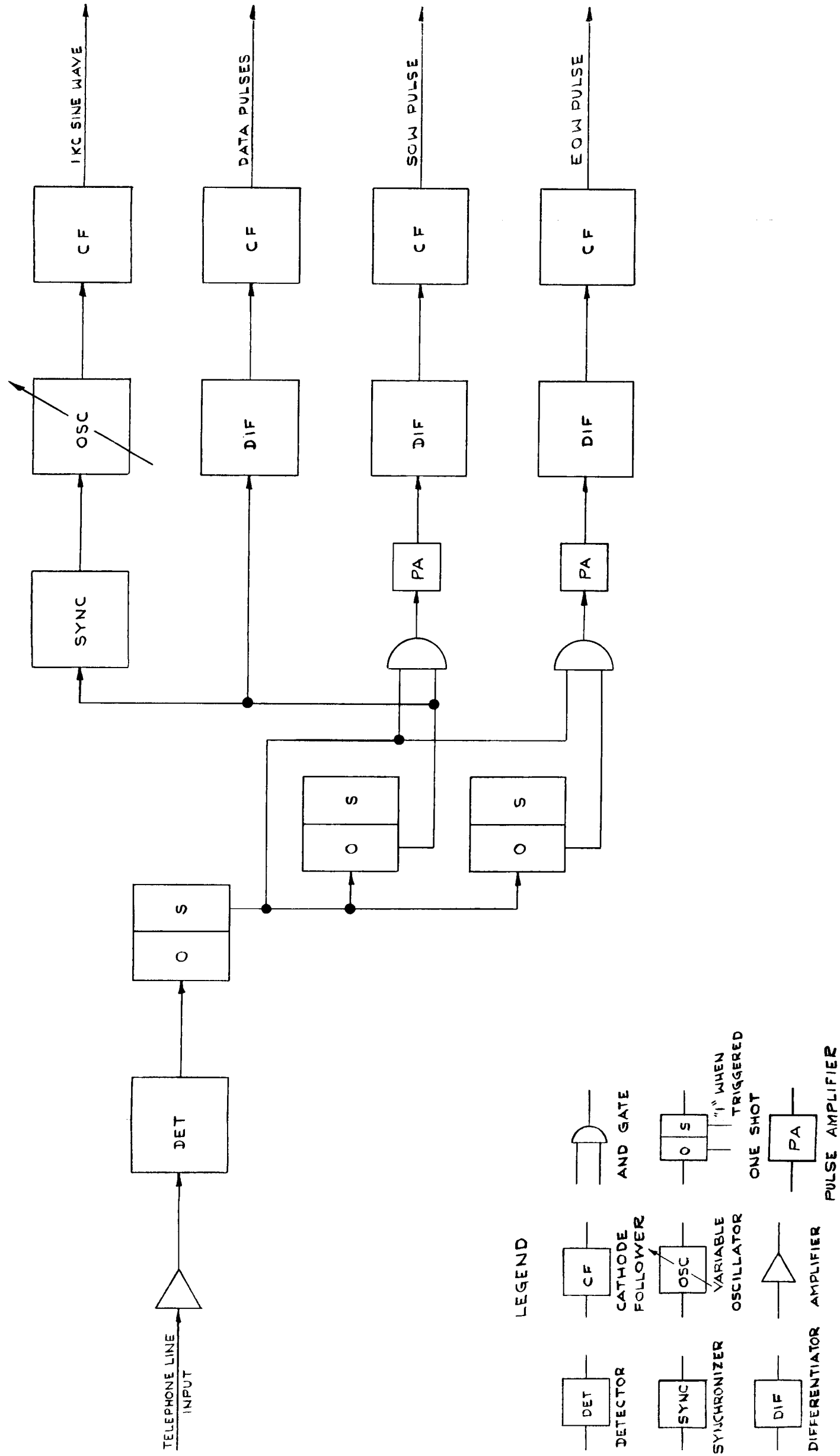
2-8.2. Level and Detection - The ideal settings for the level and detection controls



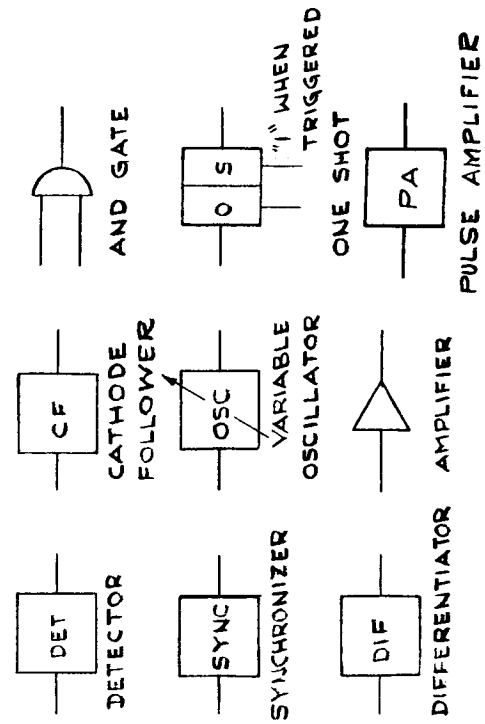
NOTE:

AMPLITUDES NOT DRAWN TO SCALE.  
 OUTPUT PULSES APPROX. 10  $\mu$ SEC. WIDE  
 AT HALF AMPLITUDE.  
 SOW & EOW BURSTS MAY VARY IN LENGTH  
 DEPENDING UPON THE SYSTEM IN WHICH  
 THEY ARE USED.  
 SOW & EOW OUTPUTS WILL NORMALLY OCCUR  
 .5 MSEC. BEFORE THE END OF BURST.  
 IN SOME SYSTEMS, SOW AND/OR EOW ARE  
 NOT NECESSARILY USED.

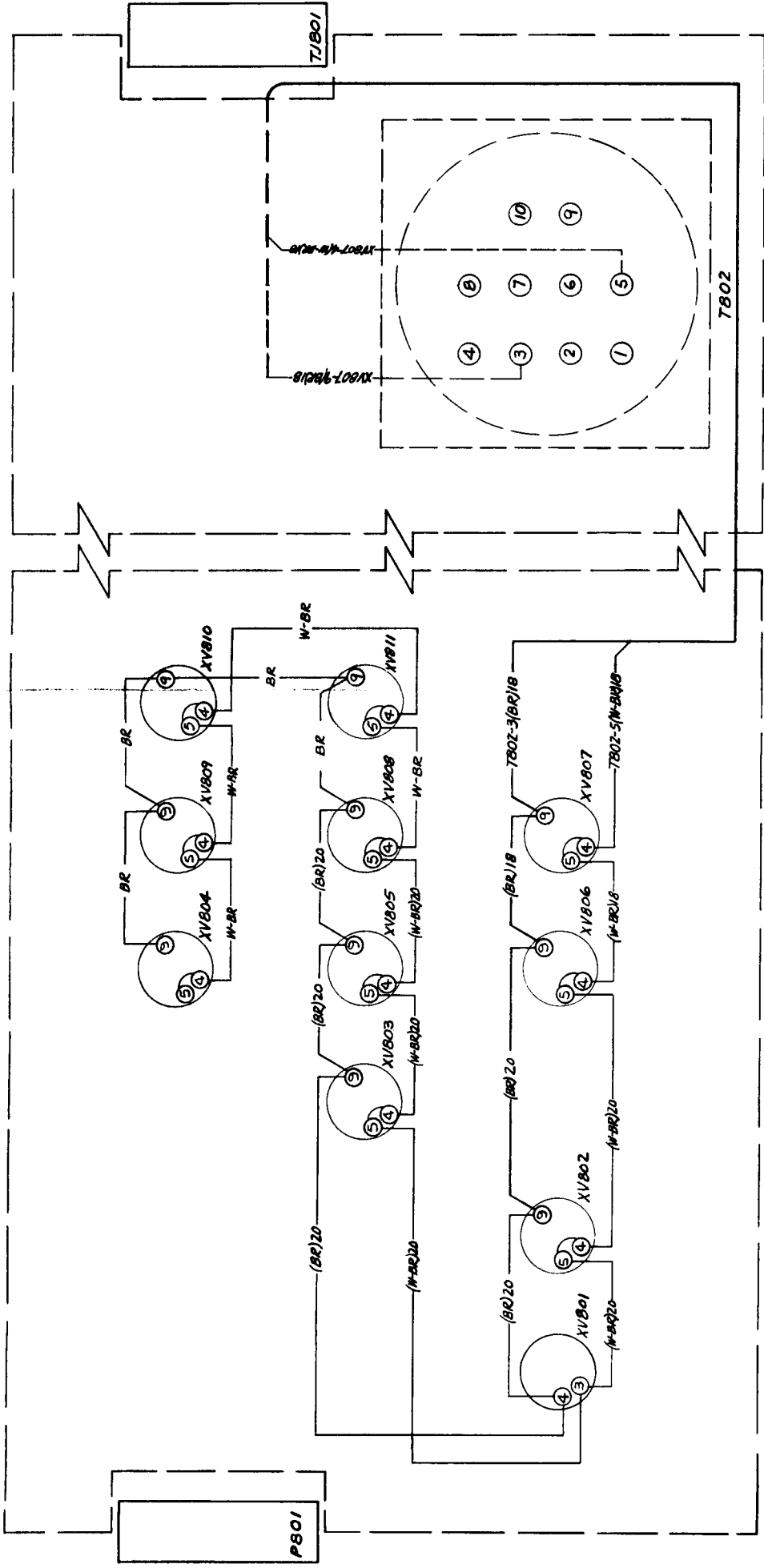




LEGEND







NOTES:

1. ALL WIRES TO BE #12 GA UNLESS SPECIFIED.
2. ALL FILAMENT WIRES TO BE TWISTED PAIRS.



## TN 28

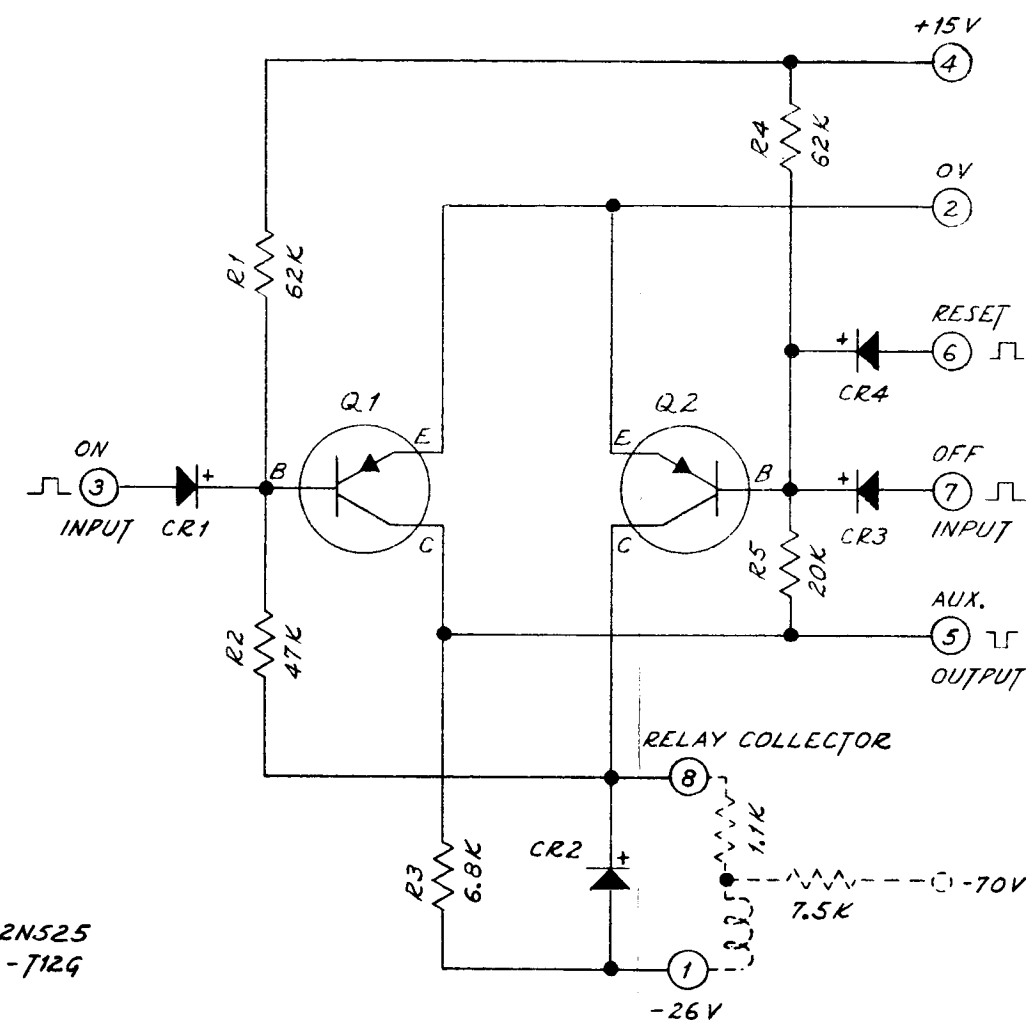
# RELAY DRIVING FLIP-FLOP

A TN28 is a bistable flip-flop which can be used for driving a relay coil or other loads of 500 ohms or more. The external load (shown on the schematic diagram in phantom between pins 8 and 1) is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" or "0" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "on" or "1" condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize. Assuming that Q1 is saturated, then its collector is approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -.05 volts; so the current through resistor R1 is approximately 0.25 milliamps. The current through the series combination of R2 and the external load resistor, which may vary from 500 ohms to 5K, varies from 0.53 to 0.48 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so this condition is a stable one. The input voltages at pins 3, 6 and 7 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +15 to 0 volts and hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This, then, is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR2 is included to suppress the voltage of an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cutoff, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and so does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil



and eliminating the voltage spike. Although the description of operation of this network has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.

Q1, Q2 - 2N525  
CR1-CR4 - 712G



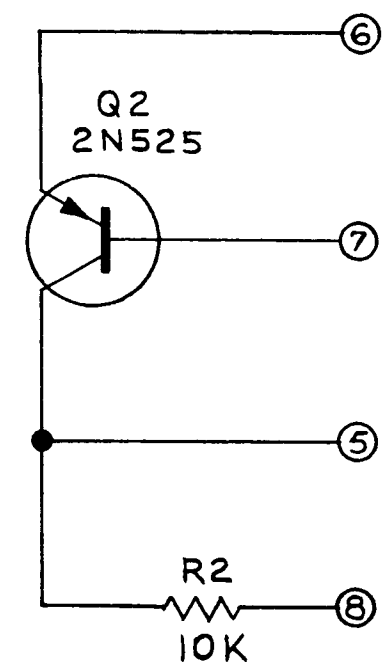
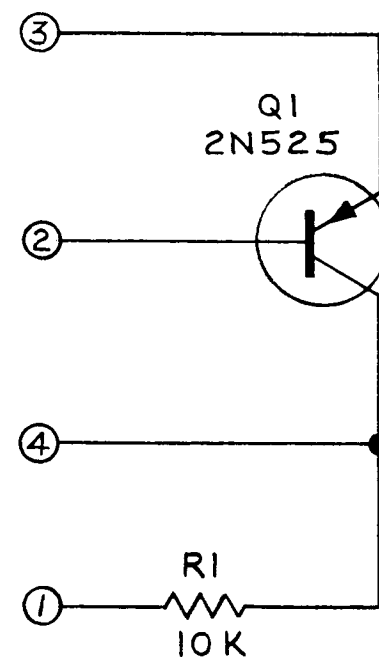
Schematic,  
TN28 Relay Driving Flip-Flop  
Dwg. #A103S28A

## **TN 57**

### **DUAL PULSE AMPLIFIER**

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.



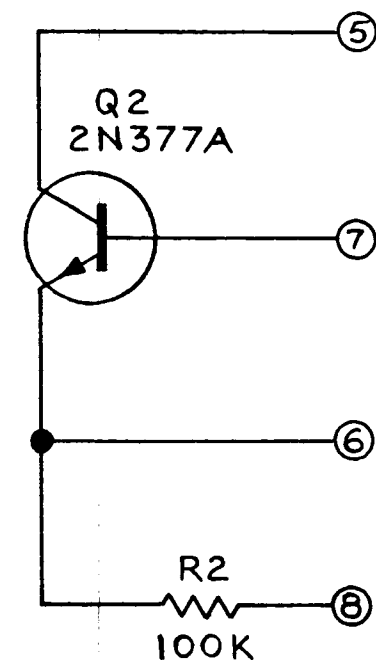
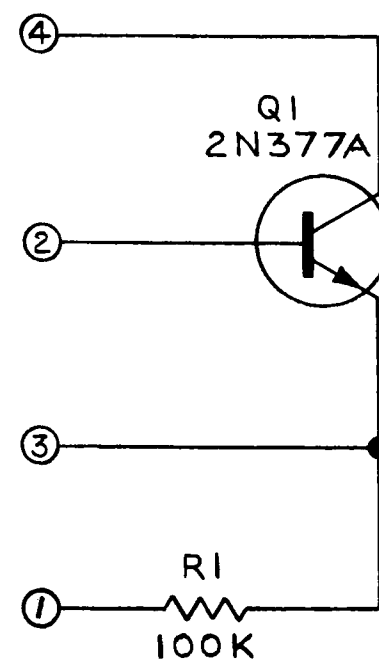
Schematic  
TN57 Dual Pulse Amplifier  
Dwg. #A103S57A

## **TN 58**

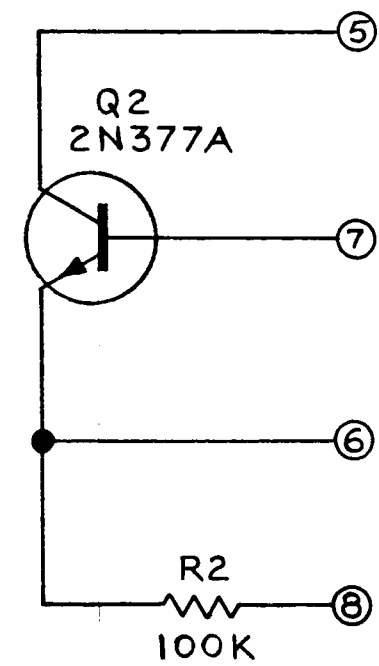
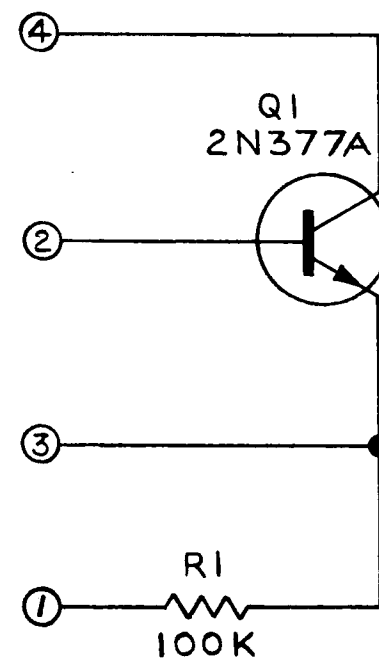
### **DUAL EMITTER FOLLOWER**

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.



Schematic  
TN58 Dual Emitter Follower  
Dwg. #A103S58A



Schematic  
TN58 Dual Emitter Follower  
Dwg. #A103S58A

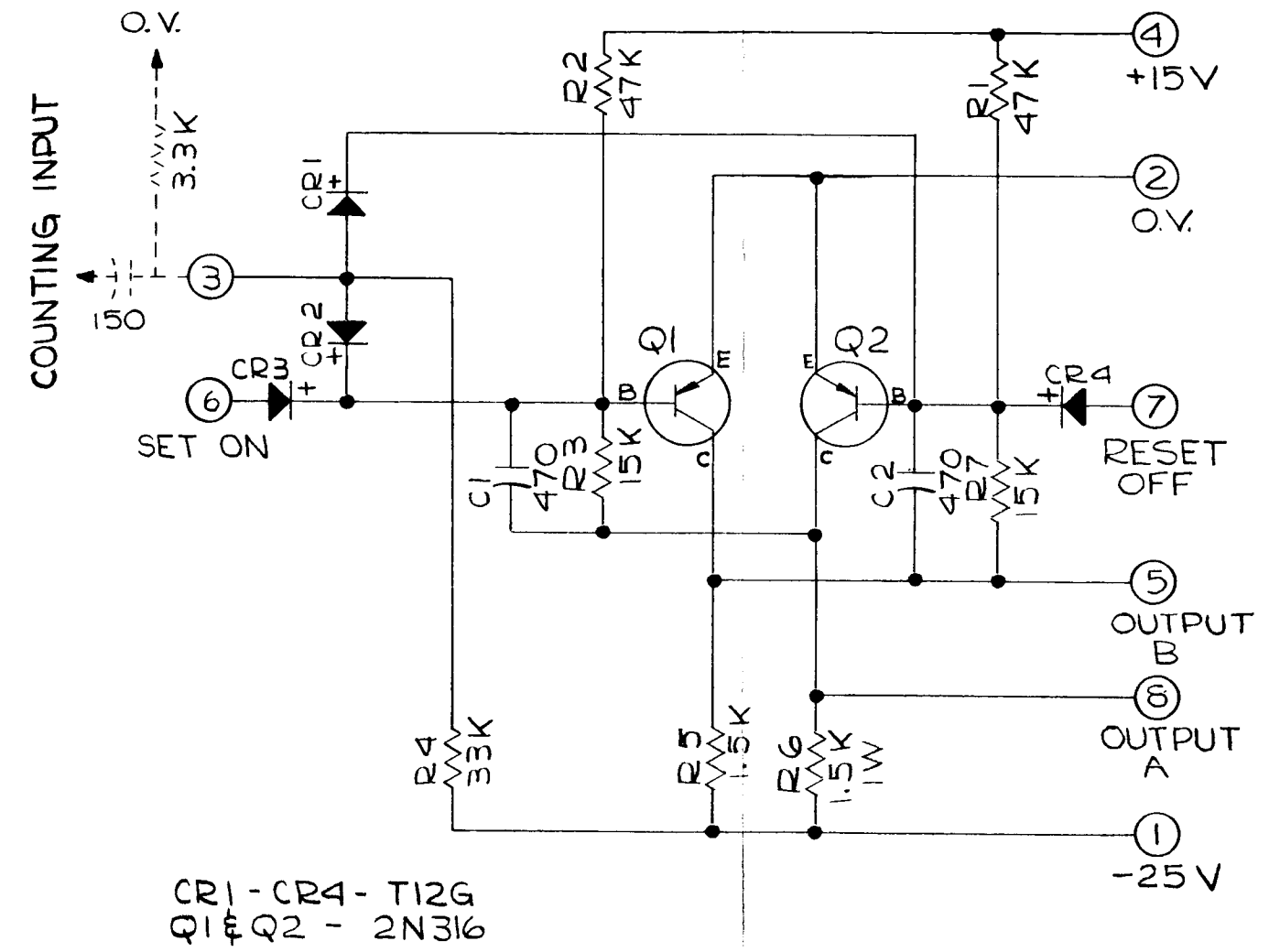
## TN 90B

### BALANCED FLIP-FLOP AND DIVIDER

The TN90B is a bistable balanced flip-flop. An auxiliary input (pin 3) allows the network to be used as a divider in a counter.

The network is defined as being in the "0" state when Q1 is saturated and Q2 is off and in the "1" state when the reverse is true. Assume that Q1 is saturated ("0" state) then the collector voltage of Q1 will be approximately 0 volts and resistor divider, R1 and R7, will maintain approximately +3.5 volts of reverse bias on the base of Q2, keeping it cut off. With Q2 cut off, resistors R3 and R6 will provide a path for Q1 base current, clamping Q1 in saturation. This condition is stable and will not be changed until an input is received on pin 3 or pin 6. Pin 6 is in "1" input, in that a positive pulse above 0 volts at pin 6 will cause CR3 to conduct, thus driving the base of Q1 positive above 0 volts, reverse biasing Q1, subsequently cutting Q1 off. As Q1 is cut off its collector will go negative and due to the resistor divider, R1 and R7, the base of Q2 will go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and due to the resistor divider of R2 and R3 the base of Q1 will be reverse biased at approximately +3.5 volts, keeping Q1 cut off, after the input pulse has passed. The network will remain in the "1" state until reset by a positive pulse on pin 7 or triggered from a pulse on pin 3, the counting input. If a positive pulse is applied on pin 3 through an external capacitor for differentiation, both Q1 and Q2 will be cut off. Capacitors C1 and C2 retain charges which are dependent upon which one of the transistors was saturated before the input pulse occurred. Since the input pulse is differentiated by a small input capacitor, it will last a very short time, less than one microsecond. At this point, the internal capacitors C1 and C2 take over, turning on the transistor that had previously been off. For example; assume the network is the "1" state, therefore Q1 is cut off and Q2 is saturated. The voltage across C1 will be approximately 3.5 volts and across C2 will be approximately 26 volts. When pin 3 goes positive above 0 volts, both bases will be driven positive, cutting the transistors off. The collector of Q2 starts to go negative from 0 volts to -23 volts. Since this occurs almost instantaneously and C1 has been charged only 3.5 volts the base of Q1 will go negative, turning Q1 on. As Q1 is turned on, Q2 is held cut off and we are now in the "0" state as explained previously. Note, since the collector of Q1 was at -23 volts before the pulse occurred on pin 3 and there wasn't any change of collector voltage when the pulse did occur. The base of Q2 would not experience any change through C2. The output pins of the network are 5 and 8. When the network is in the "0" state pin 5 will be at 0 volts and pin 8 will be approximately -23 volts and the reverse is true when the network is in the "1" state. Although the description of operation has been based on voltages of +15 volts and -25 volts this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.





Schematic,  
TN90B Balanced Flip-Flop and Divider  
Dwg. #A 103S90B

## **TN 130 B CORE DRIVER**

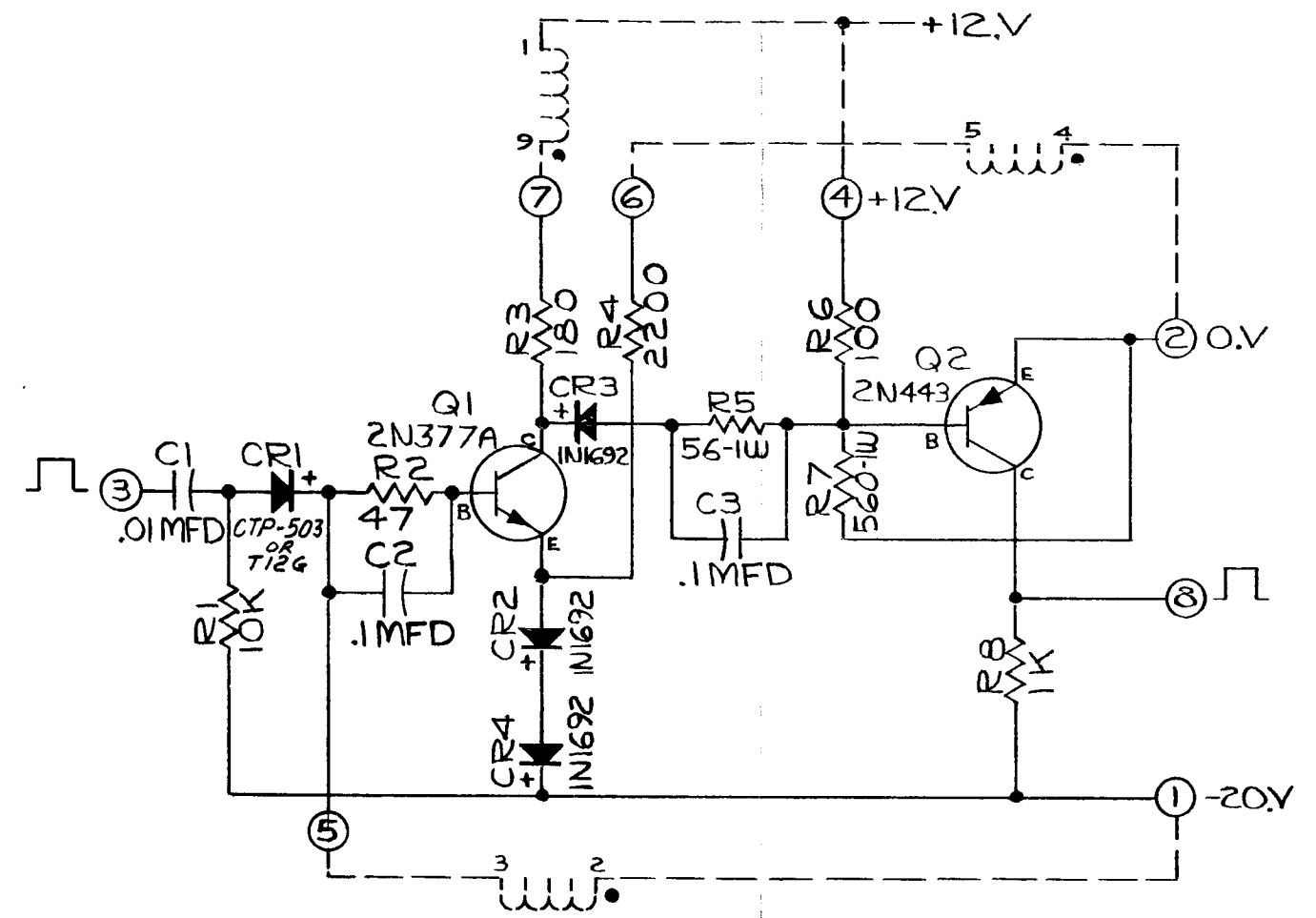
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).



NOTE:  
ALL RESISTORS  $\frac{1}{2}$  WATT  $\pm 10\%$   
UNLESS OTHERWISE NOTED.

Schematic,  
TN130B Core Driver  
Dwg. #A103S130B

## TN 138 B

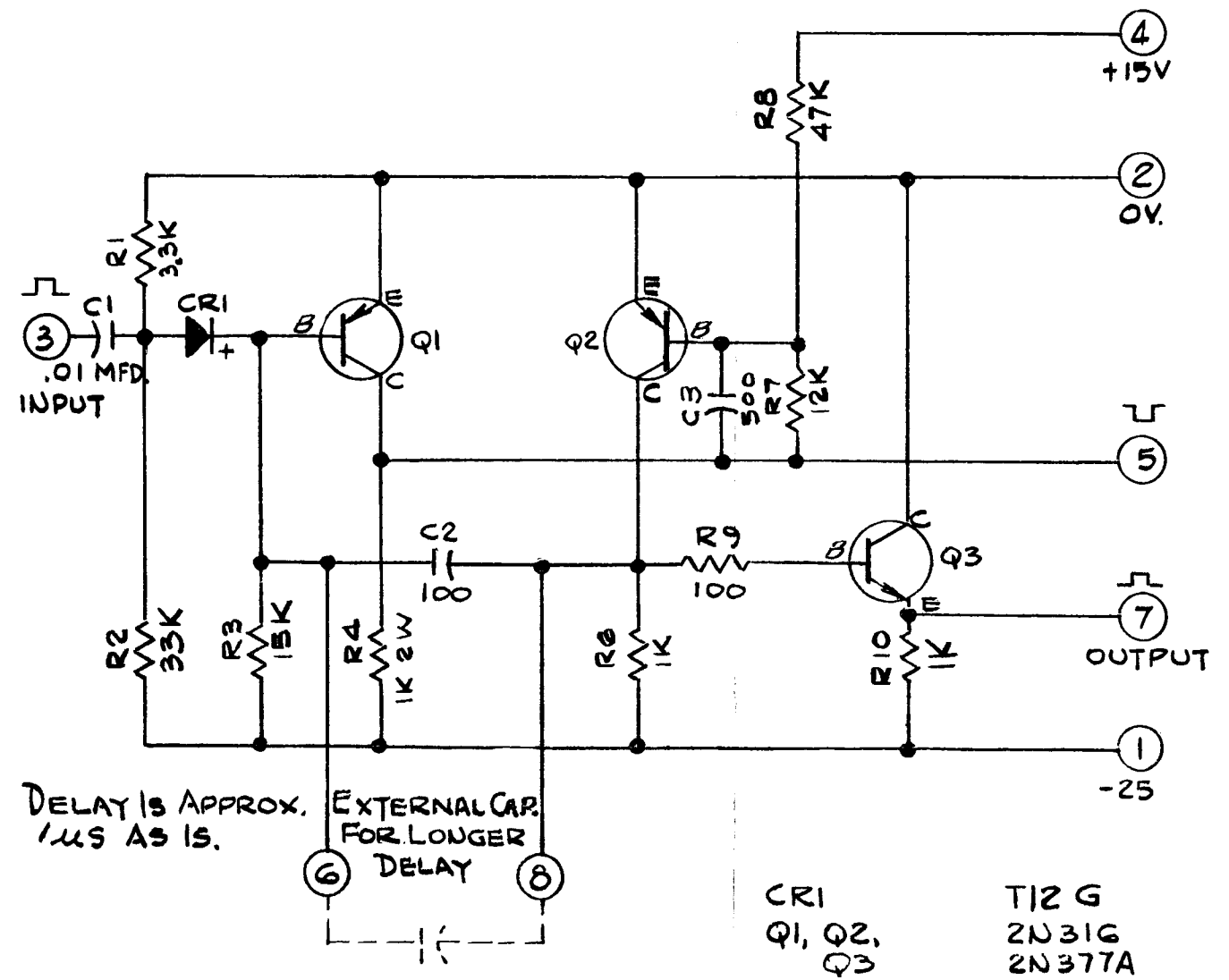
# ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138B is a one-shot (monostable multivibrator) with an emitter follower output. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated and with Q2 cut off. The base of Q1 is forward biased by R3 which is connected to -25 volts, thus saturating Q1. Since Q1 is saturated, the base of Q2 is reverse biased by the voltage divider R7 and R8 between +15 volts and the collector of Q1 (0 volts). With Q2 cut off, its collector is at approximately -25 volts; therefore the base of Q3 is at the same voltage as the emitter of Q3, keeping Q3 near cut off. Pin 7 will be at -25 volts and pin 5 will be at 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2.2 volts for protection against noise impulses. When a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -25 volts. This negative going voltage potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will now conduct, and starts to saturate rapidly. The collector of Q2 will now go positive from -25 volts to 0 volts. This voltage change, being coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive. Due to the resistor divider of R7 and R8, the base of Q2 will also go positive, reverse biasing Q2 and cutting it off. The one-shot has now returned to its quiescent condition.

The time constant of R3 and C2 determines the pulse width, which is about 1 microsecond. By adding external capacity across pins 6 and 8, the RC time constant is increased and thus the pulse width is increased. When Q2 is saturated, the base of Q3 will be positive in respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will go to 0 volts. Q3 will be in saturation as long as Q2 is in saturation. When Q2 is cut off, Q3 will be near cut off, and pin 7 will return to -25 volts.

Although the description of operation has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +10 volts and -15 volts.



Schematic,

TN138B One-Shot with Emitter Follower Output

Dwg. #A103S138B

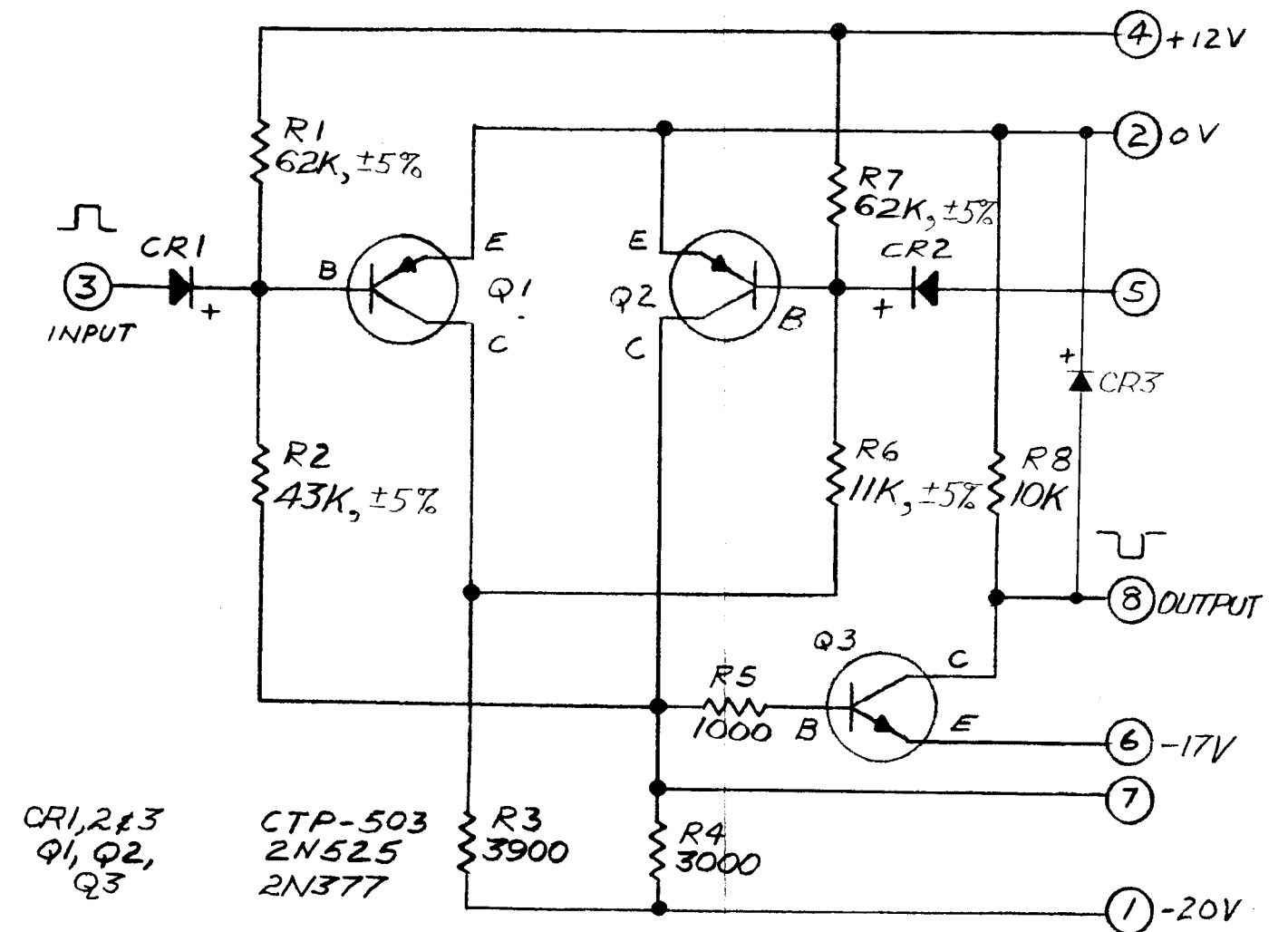
## TN 144

# FLIP-FLOP WITH PULSE AMPLIFIER OUTPUT

A TN144 is a bistable flip-flop with a pulse amplifier output which can be used to drive a load of 85 ohms or more. Since most flip-flops are limited to the amount of loading, which affects the switching of the flip-flop, a pulse amplifier has been added to permit greater loads. A transistorized neon indicator may be connected in parallel with the load to indicate the states of the flip-flop. The network is normally defined as being in the "0" state when transistor Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition when Q1 is cut off and Q2 and Q3 are saturated. Assuming that Q1 is saturated ("0" state), then its collector is at approximately -0.25 volt. Resistors R7 and R6 are then connected from +12 volts to 0 volts, and by divider action hold the base of Q2 at approximately +1.8 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -0.5 volt, so the current through resistor R1 is approximately 0.2 milliamps. Since Q2 is cut off, its collector is at approximately -19 volts, and the current through R2 and R4 is therefore 0.4 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to clamp Q1 in saturation. This mode of operation is therefore stable. Q3 is cut off when Q2 is cut off, since the base of Q3 is at -19 volts, reverse biasing the emitter. Since Q3 is cut off, there is no collector current (except for leakage) and pin 8 is at approximately 0 volts. The input voltages at pins 3 and 5 must be somewhat negative during quiescent conditions. The flip-flop may be triggered to the "1" state by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, thus raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cuts off. With Q1 cut off, R7 and R6 are no longer connected between the +12 volts and 0 volts, and Q2 is no longer clamped off. Instead, base current of Q2 may now flow through resistors R6 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +12 volts to 0 volts, and clamp the base of Q1 at approximately +5 volts, holding Q1 in a cut off condition after the input pulse passes. As Q2 is saturated and its collector goes positive, the base of Q3 goes positive enough to allow Q3 to saturate. R5 limits the base current of Q3. As Q3 saturates, pin 8 (the output pin) goes negative to approximately -17 volts. R8 is the collector load resistor of Q3, to furnish a minimum collector current when there is no external load from pin 8 of the network to 0 volts. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse on pin 5. A positive pulse (normally called reset) on pin 5 will allow base current from Q1 to be conducted through R2 and R4, driving Q1 back into saturation and restoring the initial condition. Diode CR3 is included to suppress the inductive effects of an external relay coil (if used) connected across pins 8 and 2. As Q3 goes from saturation to cut off, the relay coil is de-energized. However, the inductance of the relay coil attempts to

maintain the current through it by driving the voltage at pin 8 much more positive than 0 volts. If this were allowed to happen, Q2 could be damaged by the excessive collector-emitter voltage. During most phases of the cycle, CR3 is reverse biased; consequently, it does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven positive by the relay inductance, CR3 is forward biased and conducts, providing a path for the current through the relay coil and eliminating the excessive transient voltage to appear on the collector of Q3.





Schematic,

TN144 Flip-Flop with Pulse Amplifier Output

Dwg. #A103S144A

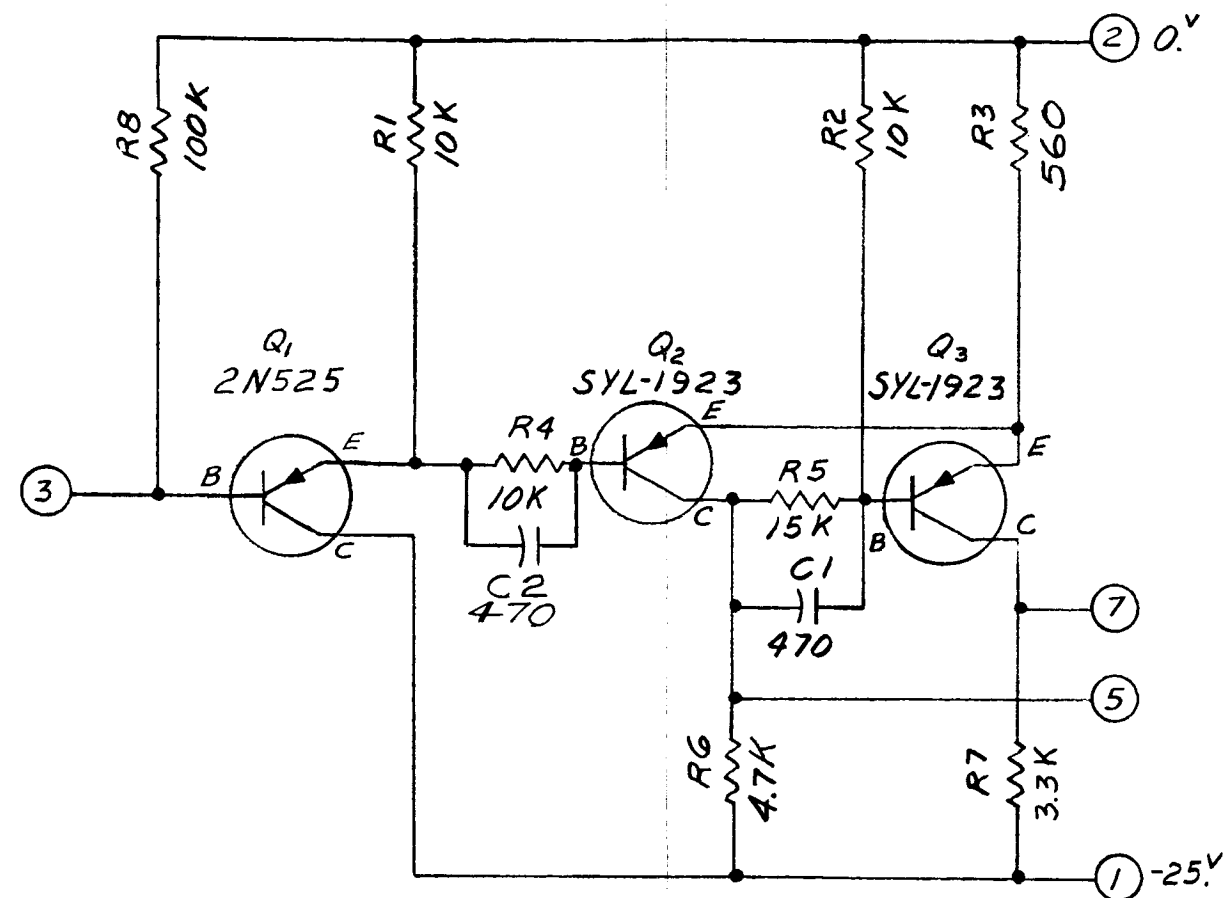
## **TN 150**

### **SCHMITT TRIGGER**

1. TN150 is a Schmitt trigger preceded by an emitter follower which presents an input impedance at approximately 70,000 ohms at pin #3. The circuit switches rapidly (in approximately 0.3 microseconds) from one state to the other with either a pulse or dc level change on pin #3 input. With the input disconnected or at a positive level, transistors Q1 and Q2 are cut-off and transistor Q3 is conducting.

2. Transistor Q1 is cut off by resistor R8 returning the base of Q1 to a more positive voltage than the emitter, and Q2 is cut-off by resistor R1 returning the base of Q2 to a more positive voltage than the emitter of Q2. The emitters of Q2 and transistor Q3 are at a negative voltage  $-E_2$  developed by the current flow through resistor R3, Q3, and resistor R7. Transistor Q3 is conducting because the base is forward biased by the resistor divider consisting of resistors R2, R5, and R6; since Q2 is cut-off. When the input, pin #3, is taken to a negative voltage, Q1 is turned on, which makes the emitter of Q1 go negative (-25 volts). This will forward bias Q2, causing it to conduct. When Q2 is conducting, the base voltage of Q3 is raised to a more positive value than the emitter voltage, thus reversing the bias on Q3 and cutting it off. This causes the collector voltage of Q3 to go from approximately -3 volts to -25 volts. Capacitor C1 is used to speed up the switching time. The outputs, pin #7 and pin #5, are opposite polarity pulses from -25 volts to -3 volts. When the output is removed or goes positive, the circuit is returned to the original state.

3. Although the description of operation has been based on power supply voltages of -25 volts, this network will operate equally well on supply voltages down to -10 volts.



NOTE:  
 1. ALL RESISTORS  $\frac{1}{2}$  WATT  $\pm 10\%$   
 UNLESS OTHERWISE SPECIFIED.  
 UNLESS OTHERWISE SPECIFIED:  
 1. Capacitance is in mmf.  
 2. Resistance is in ohms.

# MAGNETIC CORES

## 1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

## 2. THEORY OF OPERATION

### 2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on the hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

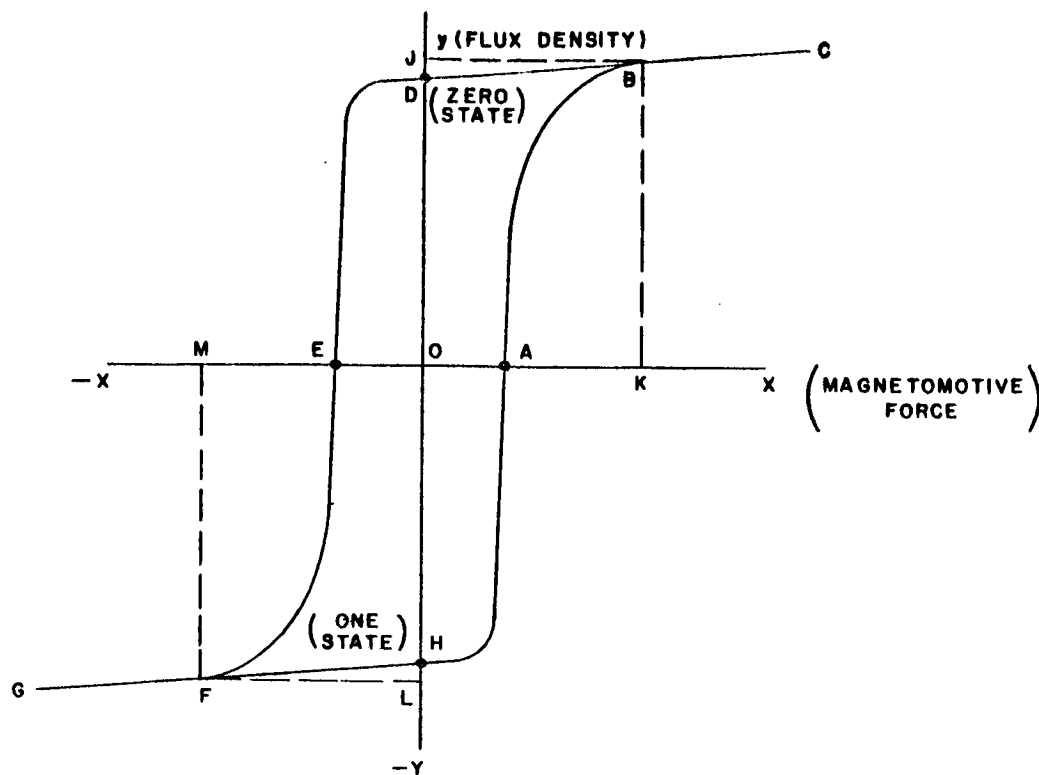


Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

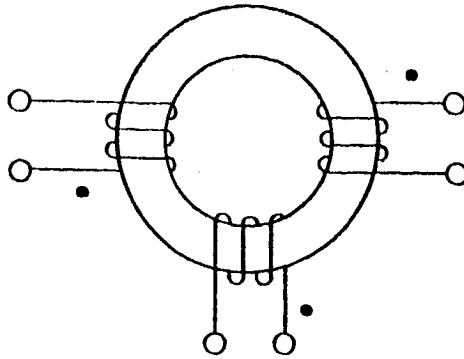


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to  $DL$ . The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

## 2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "0" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and

transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one CR3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

### 2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding

of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

## 2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.



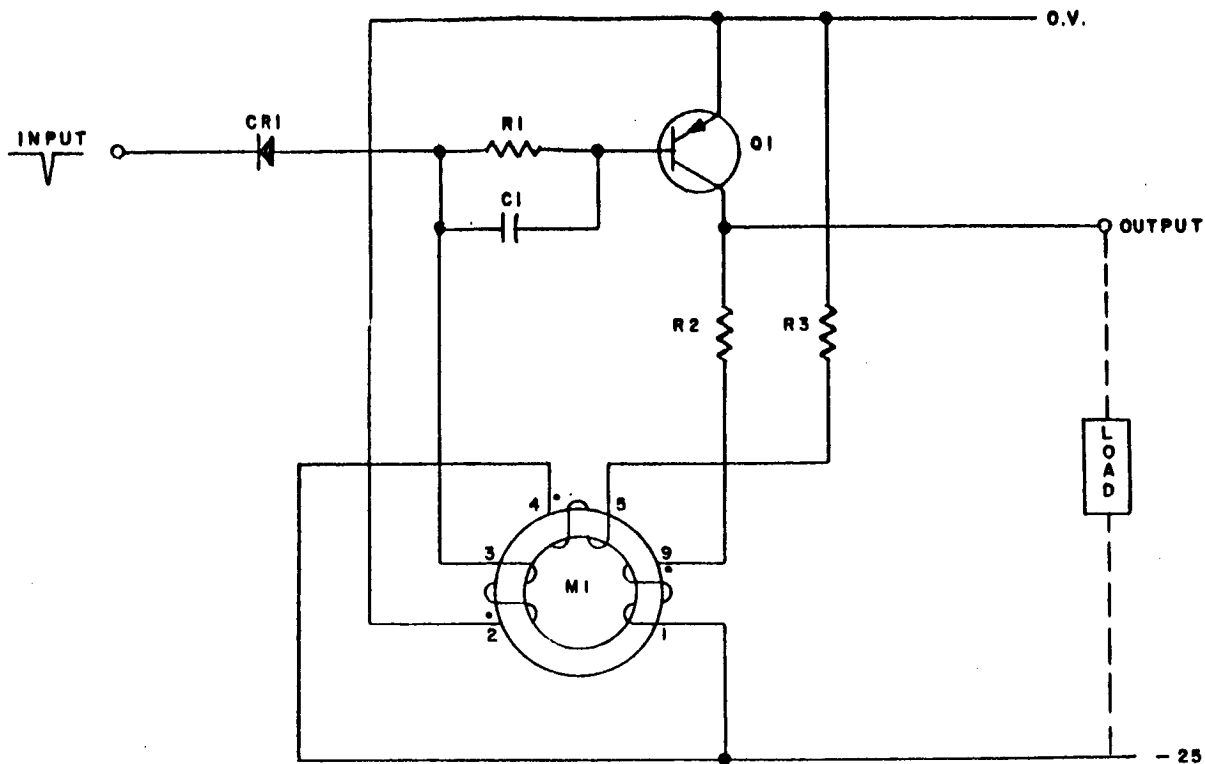


Figure MN-4. Blocking Oscillator (MN12 or MN13)

b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus

saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN13 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.

